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Analog Dialogue

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ANALOG DEVICES

Editors' Notes

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The 20-Bit DAC Is the Easiest Part of a 1-ppm-Accurate Precision Voltage Source

High precision applications require 18-bit and 20-bit, 1-ppm-accurate digital-to-analog converters, a performance level previously achieved only with cumbersome, expensive, and slow Kelvin-Varley dividers. Now, the 20-bit AD5971 DAC provides a cost-effective way to achieve 1-ppm linearity. Easy to use, it offers guaranteed specifications without requiring calibration or constant monitoring. Page 3.

Difference Amplifier Enables Low-Power, High-Performance Absolute Value

Circuit traditional precision half- and full-wave rectifiers use carefully selected high-speed op amps, fast diodes, and precision resistors, but this expensive solution suffers from crossover distortion and temperature drift. A dual-channel difference amplifier—with no external components—can provide a precision absolute value output that achieves better precision, lower cost, and lower power consumption. Page 7.

Synchronous Inverse SEPIC Topology Provides High Efficiency Buck/Boost Voltage Converters

Demand is increasing for efficient noninverting dc-to-dc converters that can operate in either buck or boost mode—with minimal cost and component count. The inverse SEPIC (single-ended primary inductor converter) is ideal for this function. An analysis of its operation and implementation with the ADP1877 dual-channel synchronous switching controller will reveal its many useful properties. Page 9.

Ultralow Distortion Audio Panpot Amplifier

An audio "panpot" circuit continuously varies the position of a monophonic audio signal between left and right channels in response to a potentiometer setting. This circuit can be built discretely, but integrating the amplifiers and resistors on a single chip offers improved specifications, less PCB area, and lower production cost. The AD8273 dual low-distortion difference amplifier uses on-chip gain-setting resistors to ensure excellent matching. Page 14.

Differential-Output Difference Amplifier System with G = ½

High-performance ADCs typically run on low-voltage supplies. To process ±10 V or larger signals, an amplifier precedes the ADC, attenuating the signal to keep it from saturating or damaging the inputs. Differential outputs are desirable to capture the full benefits of the differential-input ADC, including increased dynamic range, improved common-mode rejection, and reduced noise sensitivity. Page 15.

Full-Featured Pedometer Design Realized with 3-Axis Digital Accelerometer

Pedometers that use MEMS inertial sensors and sophisticated software to accurately detect steps can encourage individuals to get fit and lose weight. Small, low-cost, low-power MEMS sensors allow pedometers to be integrated into music players and mobile phones. This design uses an accelerometer in a full-featured pedometer that can count steps, measure distance, speed, and calories burned. Page 17.

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PRODUCT INTRODUCTIONS: VOLUME 44, NUMBER 2

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

April

ADC, sigma-delta, 4-channel, 24-bit, 4.8-kHz **AD7195**
Amplifier, difference, precision, high-voltage **AD8208**
Amplifier, operational, dual, high-speed, low distortion **ADA4898-2**
Amplifiers, operational, high-speed, rail-to-rail **ADA4891-1/ADA4891-2**
Buffer, clock fanout, SiGe, 4-output **ADCLK944**
Charge Pump, regulated 3.3-V and 5-V outputs **AD9394**
Energy Meter, polyphase, active- and reactive power **ADE7858**
Energy Meter, polyphase, active- and reactive power **ADE7868**
Energy Meter, polyphase, active power **ADE7854**
Gyroscope, yaw-rate **ADXRS623**
Mixer, active, high-linearity, 10-MHz to 6-GHz **ADL5801**
Mixer, active, integrates VCO and fractional-N PLL **ADRF6655**
Receiver, diversity, 12-bit, 8-MSPS **AD6659**
References, voltage, high-accuracy, micropower **ADR3425/ADR3450**
Regulators, switching, adjustable-output, 1.2-A **ADP2300/ADP2301**
Rheostats, digital, 1024-position, 50-time programmable **AD5174/AD5175**
Switch, high-side power, logic-level control **ADP191**
Transceiver, RF, io-homecontrol® **ADF7022**
Transceivers, HDMI, 12-bit, 225-MHz **ADV7622/ADV7623**
Transmitter, HDMI, 12-bit, 225-MHz **ADV7511**

May

Gyroscope, yaw-rate **ADXRS620**
Sensor, battery, automotive systems **ADuC7039**
Regulator, linear, low-dropout, ultralow-noise, 200-mA **ADP151**
Regulator, linear, low-dropout, 300-mA **ADP172**
Driver, LED flash, 1.5-A, I^2C-compatible **ADP1650**
Controllers, synchronous buck, 20-V **ADP1870/ADP1871**
Mixer, active, 2100-MHz to 2600-MHz **ADRF6603**
Multiplexers, analog, 2:1, 800-MHz bandwidth **ADV3219/ADV3220**
Multiplexers, analog, 4:1, 800-MHz bandwidth **ADV3221/ADV3222**
Switches, analog crosspoint, 16 × 16, 750-MHz **ADV3226/ADV3227**

June

Accelerometer, digital, 3-axis, ±2-g/±4-g/±8-g/±16-g **ADXL346**
ADC, 8-/6-/4-channel, 16-bit, simultaneous-sampling **AD7606-x**
ADC, pipelined, 16-bit, 20-MHz/40-MHz/65-MHz/80-MHz **AD9266**
ADC, sigma-delta, continuous-time, 16-bit **AD9261**
Amplifier, operational, quad, overvoltage-protection **ADA4092-4**
Amplifier, RF, 1-W, 700-MHz to 2700-MHz **ADL5604**
Amplifier, variable-gain, dual, 30-MHz **ADRF6510**
Converters, current-to-digital, 32-/64-channel, 24-bit ... **ADAS1126/ADAS1127**
Driver, clock, programmable, 10-output, LVDS **ADN4670**
Driver, gate, isolated, 2-channel, 4-A **ADuM3220**
Driver, LED, 7-channel, charge pump, funlight control **ADP8863**
Driver, LED, 7-channel, charge pump, I^2C interface **ADP8861**
Driver, line, CATV, high-power, low-distortion **ADA4320-1**
Driver, current/voltage, programmable **AD5748**
Gain Blocks, IF, 20-MHz to 1-GHz **ADL5535/ADL5536**
Gyroscope, yaw-rate, ±250°/s **ADXRS652**
Gyroscope, yaw-rate, automotive-qualified, ±50°/s **ADXRS624**
Microcontroller, precision analog, ARM7TDMI, 12-bit I/O **ADuC7122**
Microphone, MEMS, omnidirectional, analog output **ADMP401**
Microphone, MEMS, omnidirectional, digital output **ADMP421**
Mixer, active, 750-MHz to 1160-MHz **ADRF6601**
Monitor, battery safety, lithium-ion **AD8280**
Processor, SigmaDSP audio, 2-ADC/4-DAC **ADAU1401A**
Processor, SigmaDSP audio, audio-routing matrix **ADAU1442**
Processors, Blackfin® embedded **ADSP-BF52x/ADSP-BF52xC**
References, voltage high-accuracy, micropower **AD3430/AD3440**
Sensor, angular rate, high-precision **ADIS16135**
Switch, high-side power, reverse-current blocking **ADP195**
Synthesizer, frequency, fractional-N **ADF4158**
Transceiver, high-performance, narrow-band **ADF7021-V**
Transceiver, RF, 2-channel, WiMAX/BWA/WiBRO/LTE **AD9357**
Translator, clock, for base stations and optical networks **AD9553**
Transmitter, HDMI/DVI, consumer electronics control **ADV7523A**

Analog Dialogue

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The 20-Bit DAC Is the Easiest Part of a 1-ppm-Accurate Precision Voltage Source

By Maurice Egan

Introduction

A common use of high-resolution digital-to-analog converters (DACs) is providing controllable precision voltages. Applications for DACs with resolution up to 20 bits, precision up to 1 ppm, and reasonable speed include gradient coil control in medical MRI systems; precision dc sources in test and measurement; precision set-point and position control in mass spectrometry and gas chromatography; and beamprobing in scientific applications.

Over time, the definition of what constitutes a precision integrated-circuit DAC has changed rapidly as semiconductor processing and on-chip calibration technologies have advanced. Once, high-precision 12-bit DACs were considered to be hard to achieve; in recent years, 16-bit accuracy has become widely available for use in precision medical, instrumentation, and test and measurement applications; and over the horizon, even greater resolutions and accuracies are called for in control and instrumentation systems.

High precision applications for integrated circuits now require 18-bit and 20-bit, 1-ppm-accurate digital-to-analog converters, a performance level previously achieved only with cumbersome, expensive, and slow Kelvin-Varley dividers—the preserve of standards labs and hardly suitable for instrumentation systems in the field. More convenient semiconductor-based, 1-ppm-accurate solutions to such requirements using assemblies of IC DACs have been around for some years; but these complex systems use many devices, require frequent calibrations and great care to achieve accuracy, and are both bulky and costly (see Appendix). The precision instrumentation market has long needed a simpler, cost-effective DAC that doesn't require calibration or constant monitoring, is easy to use, and offers guaranteed specifications. A natural evolution from 16-bit and 18-bit monolithic converters—such a DAC is now a reality.

The AD5791 1-ppm DAC

Advances in semiconductor processing, DAC architecture design, and fast on-chip calibration techniques make possible highly linear, stable, fast-settling digital-to-analog converters that deliver better than 1-ppm relative accuracy, 0.05-ppm/°C temperature drift, 0.1-ppm p-p noise, better than 1-ppm long-term stability, and 1-MHz throughput. These small, single chip devices have guaranteed specifications, do not require calibration, and are easy to use. A typical functional diagram for the AD5791 and its companion reference- and output buffers is shown in Figure 1.

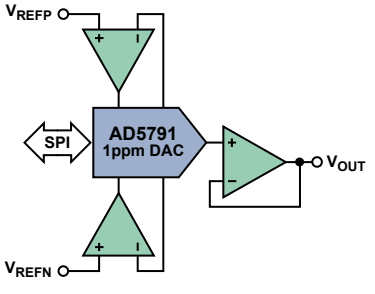

Figure 1. AD5791 typical operating block diagram.

The AD5791 single-chip, 20-bit, voltage-output digital-to-analog converter specifies 1-LSB (*least-significant bit*) *integral nonlinearity* (INL) and *differential nonlinearity* (DNL), making it the world's first monolithic 1-ppm-accurate digital-to-analog converter (1 LSB at 20 bits is one part in 2^{20} = one part in 1,048,576 = 1 ppm). Designed for use in high-precision instrumentation and test and measurement systems, it offers a significant leap in all-around performance compared to other solutions, providing greater levels of accuracy and repeatability in less space and at lower cost, permitting instrumentation applications that previously would not have been economically feasible.

Its design, shown in Figure 2, features precision voltage-mode R-2R architecture, exploits state-of-the-art thin-film resistor-matching techniques, and employs on-chip calibration routines to achieve 1-ppm accuracy levels. Because the device is factory calibrated and, therefore, requires no run-time calibration routines, its latency is no greater than 100 ns, so the AD5791 can be used in waveform-generation applications and fast control loops.

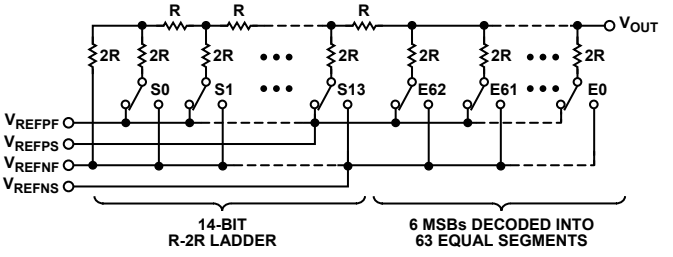

Figure 2. DAC ladder structure.

Besides its impressive linearity, the AD5791 combines 9 nV/$\sqrt{\text{Hz}}$ noise density, 0.6-μV peak-to-peak noise in the 0.1-Hz to 10-Hz frequency band, 0.05-ppm/°C temperature drift, and better than 0.1-ppm long-term stability over 1000 hours.

A high-voltage device, it operates from dual supplies of up to ±16.5 V. The output voltage span is set by the applied positive and negative reference voltages, V_{REFP} and V_{REFN}, offering a flexible choice of output range.

The precision architecture of the AD5791 requires high-performance external amplifiers to buffer the reference source from the 3.4 kΩ DAC resistance and facilitate force-sensing at the reference input pins to ensure the AD5791's 1-ppm linearity. An output buffer is required for load driving to unburden the 3.4 kΩ output impedance of the AD5791—unless a very high-impedance, low-capacitance load is being driven—or attenuation is tolerable and predictable.

Because the amplifiers are external, they can be selected to optimize for noise, temperature drift, and speed—and the scale factor can be adjusted—depending on the needs of the application. For the reference buffers, the AD8676 dual amplifier is recommended, based on its low noise, low offset error, low offset error drift, and low input bias currents. The input bias current specification of the reference buffers is important, as excessive bias currents will degrade the dc linearity. The degradation of integral nonlinearity, in ppm, as a function of input bias current, is typically:

$$Extra\ INL\ Error = \frac{0.2 \times I_{BIAS}}{(V_{REFP} - V_{REFN})^2}$$

where I_{BIAS} is in nA; V_{REFP} and V_{REFN} are in volts. For example, with a ±10-V reference input span, an input bias current of 100 nA will increase the INL by 0.05 ppm.

The key requirements for an output buffer are similar to those for the reference buffers—except for bias current, which does not affect the AD5791's linearity. Offset voltage and input bias current can affect output offset voltage, though. To maintain dc precision, the AD8675 is recommended as an output buffer. High-throughput applications require a fast output buffer amplifier with higher slew rate.

Table 1 lists the key specifications of a few appropriate precision amplifiers.

The AD5791 offers reduced design time, reduced design risk, reduced cost, reduced board size, increased reliability, and guaranteed specifications.

Figure 3 is a circuit schematic implementing the AD5791 (U1) as a precision digitally controlled 1-ppm voltage source with a ±10 V range in 20-µV increments using the AD8676 (U2) as reference buffers and the AD8675 (U3) as the output buffer. The absolute accuracy is determined by the choice of the external 10 V references.

Performance Measures

The important measures of this circuit are integral nonlinearity, differential nonlinearity, and 0.1-Hz to 10-Hz peak-to-peak noise. Figure 4 shows that typical INL is within ±0.6 LSB.

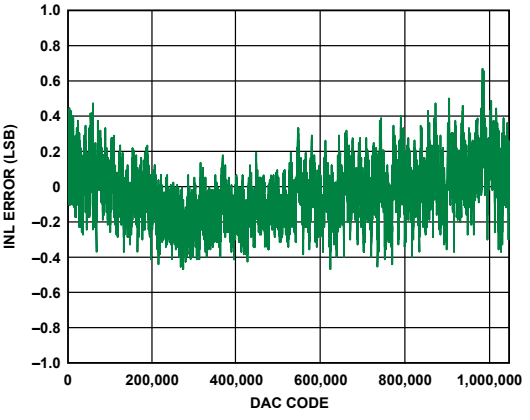

Figure 4. Integral nonlinearity plot.

Figure 5 shows a typical DNL of ±0.5 LSB; the output is guaranteed monotonic over the entire range of bit transitions.

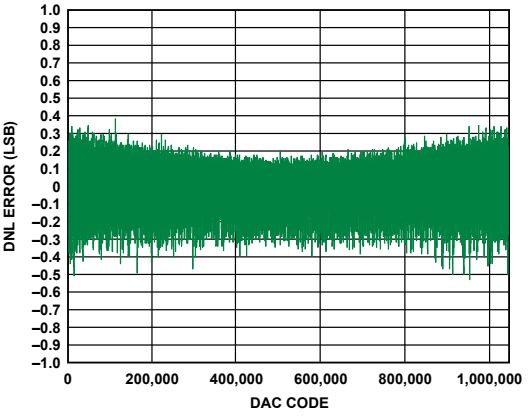

Figure 5. Differential nonlinearity plot.

Peak-to-peak noise in the 0.1-Hz to 10-Hz bandwidth is about 700 nV, as shown in Figure 6.

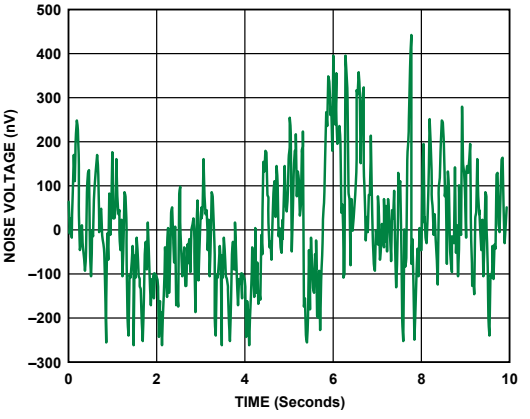

Figure 6. Low-frequency noise.

Table 1. Precision Amplifier Key Specifications

	Noise Spectral Density	1/f p-p Noise (0.1 Hz to 10 Hz)	Offset Voltage Error	Offset Voltage Error Drift	Input Bias Current	Slew Rate
AD8675/AD8676	2.8 nV/√Hz	0.1 µV	10 µV	0.2 µV/°C	0.5 nA	2.5 V/µs
ADA4004-1	1.8 nV/√Hz	0.1 µV	40 µV	0.7 µV/°C	40 nA	2.7 V/µs
ADA4898-1	0.9 nV/√Hz	0.5 µV	20 µV	1 µV/°C	100 nA	55 V/µs

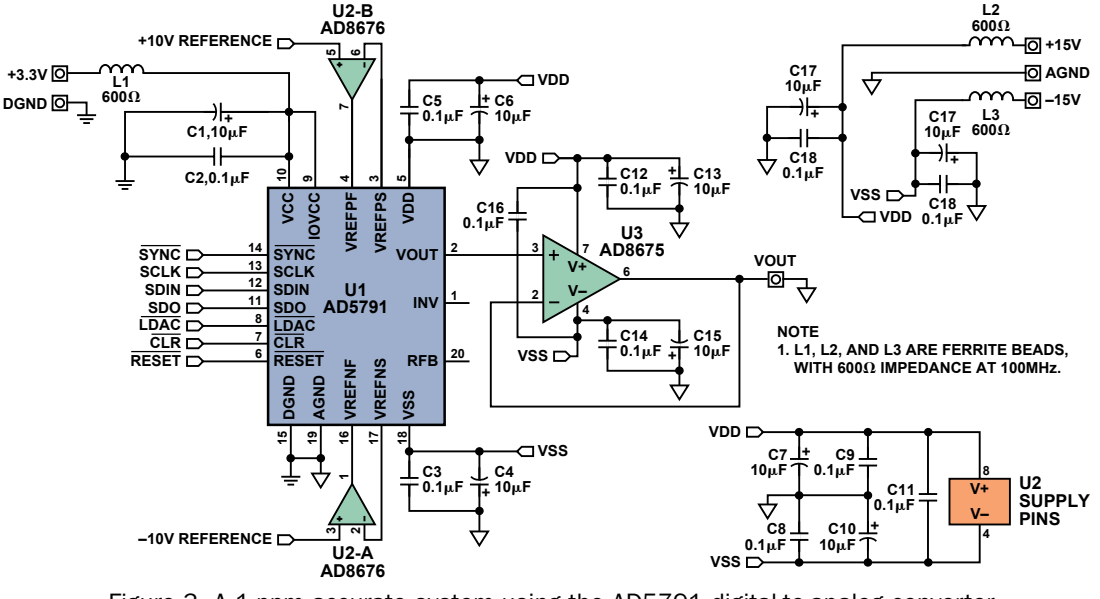

Figure 3. A 1-ppm accurate system using the AD5791 digital-to-analog converter.

The AD5791 Is Only the Beginning: 1-ppm Circuit Complexities

Even though precision sub-1-ppm components such as the AD5791 are available on the market, building a 1-ppm system is not a task that should be taken lightly or rushed into. Error sources that show up at this level of precision must be carefully considered. The major contributors to errors in 1-ppm-accurate circuits are noise, temperature drift, thermoelectric voltages, and physical stress. Precision circuit construction techniques should be followed to minimize the coupling and propagation of these errors throughout the circuit and the introduction of external interference. These considerations will be summarized here briefly. Further information can be found in the References.

Noise

When operating at 1-ppm resolutions and accuracies, it is of utmost importance to keep noise levels to a minimum. The noise spectral density of the AD5791 is 9 nV/$\sqrt{\text{Hz}}$, mostly from the Johnson noise of the 3.4-kΩ DAC resistance. All peripheral components should have smaller noise contributions to minimize increases to the system noise level. Resistor values should be less than the DAC resistance to ensure that their Johnson noise contribution will not significantly add to the root-sum-square overall noise level. The AD8676 reference buffers and the AD8675 output buffer have a specified noise density of 2.8 nV/$\sqrt{\text{Hz}}$, well below the DAC's contribution.

High-frequency noise can be eliminated relatively easily with simple R-C filters, but low-frequency 1/f noise in the 0.1-Hz to 10-Hz range cannot be easily filtered without affecting dc accuracy. The most effective method of minimizing 1/f noise is to ensure that it is never introduced into the circuit. The AD5791 generates about 0.6 μV p-p of noise in the 0.1-Hz to 10-Hz bandwidth, well below the 1-LSB level (1 LSB = 19 μV for a ±10-V output span). The target for maximum 1/f noise in the entire circuit should be about 0.1 LSB, or 2 μV; this can be ensured through proper component choice. The amplifiers in the circuit generate 0.1-μV p-p 1/f noise; the three amplifiers in the signal chain generate a total of approximately 0.2-μV p-p noise at the circuit output. Add this to the 0.6-μV p-p from the AD5791, and the total expected 1/f noise is about 0.8 μV p-p, a figure that closely correlates with the measurement displayed in Figure 5. This offers adequate margin for other circuitry that may be added, such as amplifiers, resistors, and a voltage reference.

Besides random noise, it is important to avoid errors caused by radiated, conducted, and induced electrical interference. Such techniques as shielding, guarding, and scrupulous attention to grounding and proper printed-circuit-board wiring techniques are imperative.

Temperature Drift

As with all precision circuits, drift of all components with temperature is a major source of error. The key to minimizing the drift as much as possible is to choose critical components with sub-1-ppm temperature coefficients. The AD5791 exhibits a very low 0.05-ppm/°C temperature coefficient. The AD8676 reference buffers drift at 0.6 μV/°C, introducing an overall 0.03-ppm/°C gain drift into the circuit; the AD8675 output buffer contributes a further 0.03-ppm/°C output drift; this all adds up to a figure of 0.11 ppm/°C. Low drift, thermally matched resistor networks should be used for scaling and gain circuits. Vishay bulk metal-foil voltage-divider resistors, series 300144Z and 300145Z, with a temperature coefficient of resistance tracking to 0.1 ppm/°C, are recommended.

Thermoelectric Voltages

Thermoelectric voltages are the result of the Seebeck effect: temperature-dependent voltages are generated at dissimilar metal junctions. Depending on the metallic components of the junction, the generated voltage can be anywhere from 0.2 μV/°C to 1 mV/°C. The best case, a copper-to-copper junction, will generate less than 0.2 μV/°C of thermoelectric EMF. In the worst case, copper-to-copper-oxide can generate up to 1 mV/°C of thermoelectric voltage. This sensitivity to even small temperature fluctuations means that nearby dissipative elements or slow-moving air currents crossing over a printed circuit board (PCB) can create varying temperature gradients, which in turn generate varying thermoelectric voltages that are manifested as a low-frequency drift similar to low-frequency 1/f noise. Thermoelectric voltages can be avoided by ensuring that there are no dissimilar junctions in the system and/or eliminating thermal gradients. While it is virtually impossible to eliminate dissimilar metal junctions—many different metals exist in IC packaging, PCB circuits, wiring, and connectors—keeping all connections clean and oxide-free will go a long way to keeping thermoelectric voltages low. Enclosing the circuit to shield circuitry from air currents would be an effective thermoelectric voltage stabilizing method, and it could have the added value of providing electrical shielding. Figure 7 shows the difference in voltage drifts between a circuit that is open to air currents and one that is enclosed.

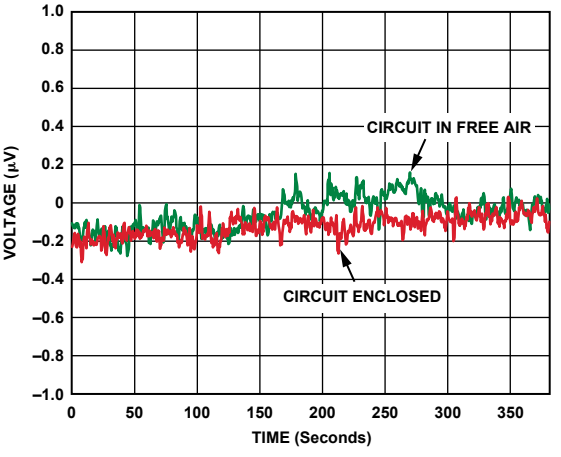

Figure 7. Voltage drift vs. time for open- and enclosed systems.

To cancel out the thermoelectric voltages, compensating junctions could be introduced into the circuit, a task that would involve considerable trial and error and iterative testing to ensure the correct pairing and positions of the inserted junctions. By far the most efficient method is to *reduce* the number of junctions in the circuit by minimizing component count in the signal path and stabilizing the local and ambient temperatures.

Physical Stress

High-precision analog semiconductor devices are sensitive to stress on their package. Stress relief compounds used within the packaging have a settling effect, but they cannot compensate for significant stress due to pressure exerted directly on the package by local sources, such as flexing of the PCB. The larger the printed circuit board, the more stress that a package could potentially suffer, so sensitive circuitry should be placed on as small a board as possible—with connection to the larger system through flexible or nonrigid connectors. If a large board cannot be avoided, stress relief cuts should be made around sensitive components, on two or (preferably) three sides of the component, greatly reducing the stress on the component due to board flexing.

Long-Term Stability

After noise and temperature drift, long-term stability deserves consideration. Precision analog ICs are very stable devices but do undergo long-term age-related changes. Long-term stability for the

AD5791 is typically better than 0.1 ppm/1000 hours at 125°C. The aging is not cumulative but follows a square root rule (if a device ages at 1 ppm/1000 hours, it ages at $\sqrt{2}$ ppm/2000 hours, $\sqrt{3}$ ppm/3000 hours, …), and the time is typically 10 times longer for each 25°C reduction in temperature; so, at 85°C operation, one can expect aging of 0.1 ppm over a 10,000 hour period, approximately 60 weeks. If this is extrapolated, 0.32 ppm aging can be expected over a 10-year period, so the data sheet dc specifications can be expected to drift by 0.32 ppm over a 10-year period when operating at 85°C.

Circuit Construction and Layout

In a circuit where such a high level of accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the PCB such that the analog and digital sections are separated and confined to separate areas of the board. If the DAC is in a system where multiple devices require an analog-to-digital ground connection, establish the connection at one point only. Establish the star-point ground as close as possible to the device. There should be ample power supply bypassing of 10 μF in parallel with 0.1 μF on each supply terminal, as close to the package as possible, ideally right up against the device. The 10-μF capacitors should be of the tantalum bead type. The 0.1-μF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESL), such as the common multilayer ceramic types—to provide a low-impedance path to ground at high frequencies to handle transient currents due to internal logic switching. A series ferrite bead on each power supply line will further help to block high-frequency noise from getting through to the device.

The power supply traces should be as large as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line. Shield fast-switching signals, such as clocks, with digital ground to avoid radiating noise to other parts of the board. They should never be run near the reference inputs or under the package. It is essential to minimize noise on the reference inputs because it couples right through to the DAC output. Avoid crossover of digital and analog signals, and run traces on opposite sides of the board at right angles to each other to reduce the effects of feedthrough on the board.

Voltage Reference

Holding the performance of the entire circuit firmly within its grasp is the external voltage reference; its noise and temperature coefficient directly impact the system's absolute accuracy. To capitalize on the challenge posed by the 1-ppm AD5791 digital-to-analog converter, the reference and associated components should have temperature drift and noise specifications comparable to those of the DAC. Although a reference with temperature drift of 0.05 ppm/°C is nothing short of fantasy, 1 ppm/°C and 2 ppm/°C voltage references with 0.1-Hz to 10-Hz noise of less than 1 μV p-p do exist.

Conclusion

As the accuracy requirements of precision instrumentation—and test and measurement applications—increase, more accurate components are being developed to meet these needs. They have guaranteed precision specifications at the 1-ppm level without further user calibration and are easy to use. However, when designing circuitry for this level of precision, one must bear in mind the many environmental and design-related challenges that exist. Successful precision-circuit performance will come as a result of considering and understanding these challenges and making correct component choices.

References

(Information on all ADI components can be found at www.analog.com.)

1. "The Long Term Stability of Precision Analog ICs, or How to Age Gracefully and Avoid Sudden Death." Analog Devices. R*arely Asked Questions*. http://www.analog.com/en/analog-microcontrollers/analog-microcontrollers/products/rarely-asked-questions/RAQ_precisionAnalogICs/resources/fca.html.
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Author

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Appendix

Figure 8 shows a block diagram of a typical contemporary 1 ppm DAC solution. The core of the circuit consists of two 16-bit digital-to-analog converters—a major DAC and a minor DAC—the outputs of which are scaled and combined to yield an increased resolution. The major DAC output is summed with the attenuated minor DAC output so that the minor DAC fills the resolution gaps between the major DAC's LSB steps.

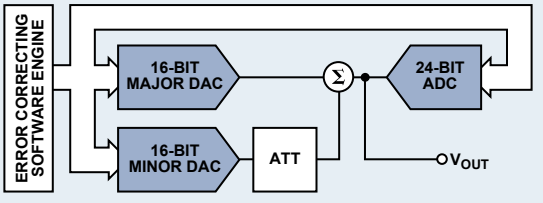

Figure 8.

The combined DAC outputs need to be monotonic, but not extremely linear, because high performance is achieved with constant voltage feedback via a precision analog-to-digital converter, which corrects for the inherent component errors; thus, the circuit accuracy is limited by the ADC rather than the DACs. However, because of the requirement for constant voltage feedback and the inevitable loop delay, the solution is slow, potentially requiring seconds to settle.

Although this circuit can, with significant endeavor, ultimately achieve 1 ppm accuracy, it is complex to design, likely to require multiple design iterations, and requires a software engine and precision ADC to achieve accuracy. To guarantee 1-ppm accuracy the ADC will also require correction—since an ADC with guaranteed 1-ppm linearity is not available. The simple block diagram of Figure 8 illustrates the concept, but the actual circuit in reality is far more complex, with multiple gain, attenuation, and summing stages, involving many components. Also required is significant digital circuitry to facilitate the interface between both DACs and the ADC—not to mention the software required for error correction.

More Value from Your Absolute Value Circuit—Difference Amplifier Enables Low-Power, High-Performance Absolute Value Circuit

By Moshe Gerstenhaber and Reem Malik

Precision half- and full-wave rectifiers are traditionally built using carefully selected components, including high speed op amps, fast diodes, and precision resistors. The high component count makes this solution expensive, and it suffers from crossover distortion and temperature drift variation between components.

This article shows how a dual-channel difference amplifier can be configured—with no external components—to provide a precision absolute value output. This innovative approach can achieve better precision, lower cost, and lower power consumption than conventional approaches.

A difference amplifier[1] comprises an op amp and four resistors configured as a subtractor, as shown in Figure 1. Featuring laser-wafer-trimmed resistors, low-cost monolithic difference amplifiers offer very high gain accuracy, low offsets, low offset drift, high common-mode rejection, and better overall performance than discrete alternatives.

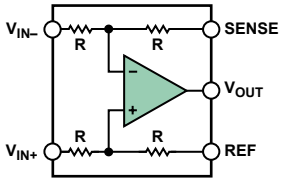

Figure 1. Difference amplifier.

Traditional Absolute Value Circuit

Figure 2 shows a schematic of a commonly used full-wave rectifier circuit. To achieve high performance, this design relies on two fast op amps and five precision resistors. When the input signal is positive, the output of A1 is negative, so D1 is reverse biased. D2 is forward-biased, closing the feedback loop around A1 through R2 and forming an inverting amplifier. A2 sums the output of A1 times a gain of −2 with the input signal times a gain of −1, leaving a net gain of +1. When the input signal is negative, D1 is forward-biased, closing the feedback loop around A1. D2 is reverse-biased and does not conduct. A2 inverts the input signal, resulting in a positive output. Thus, the output of A2 is a positive voltage that represents the absolute value of the input, whether positive or negative.

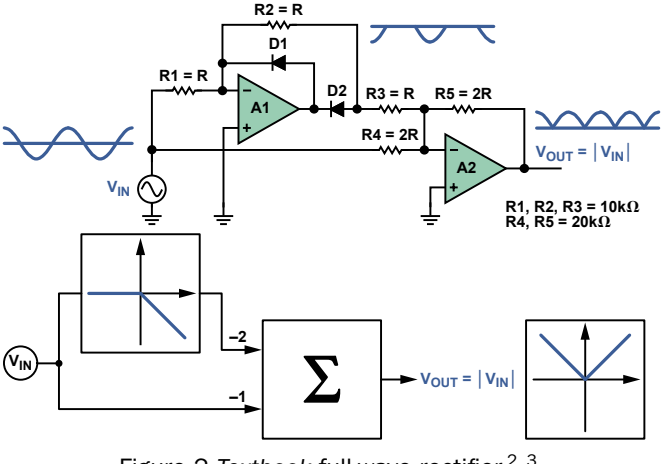

Figure 2. *Textbook* full-wave rectifier.[2, 3]

This design has several inherent performance and system shortcomings, including cost, crossover distortion, gain error, and noise. The design requires *dual power supplies* and many high performance components, further increasing the cost and complexity. The response time can be long because A1's output has to swing from $-V_{BE}$ to $+V_{BE}$ as the input signal crosses from 0 V + ΔV to 0 V – ΔV. High speed op amps and diodes can help mitigate this problem, but only at the cost of increased power dissipation. The gain accuracy of the absolute value output is determined by the matching of R1, R2, R3, R4, and R5. A substantial error between the positive and negative absolute value peaks will occur if even a single resistor is mismatched by a small amount. The overall noise gain is 6, amplifying the effects of op-amp noise, offset, and drift.

Improved Absolute Value Circuit

Figure 3 shows a simpler, more effective absolute value circuit that requires only one AD8277[4] dual-channel difference amplifier and a *single positive supply*. When the input signal is positive, A1 acts as a voltage follower. Both inputs of A2 are at the same potential as the input signal, so A2 simply passes the positive signal to the output. When the input signal is negative, the output of A1 is at 0 V, and A2 inverts the input signal. The overall result is the absolute value of the input signal. Signals as large as ±10 V can be rectified at frequencies as high as 10 kHz. If the signal to be rectified is very small, a pull-down resistor at each op-amp output can improve the circuit performance around 0 V.

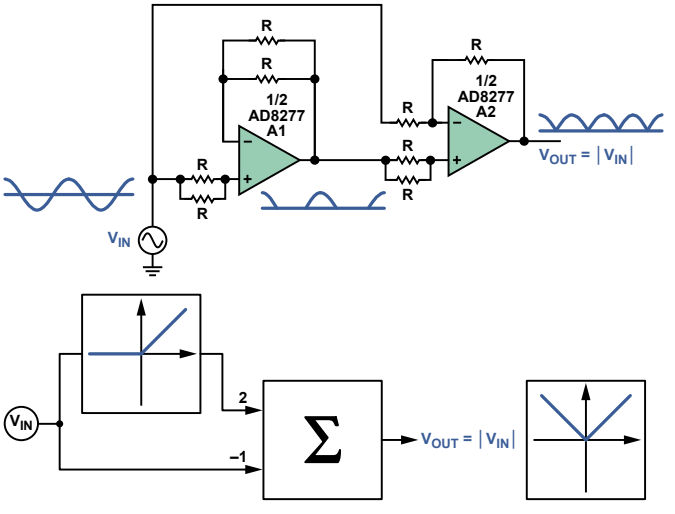

Figure 3. Single-supply absolute value circuit using AD8277.

The function of this circuit, while deceptively simple, is possible only because of the AD8277's exceptional input and output characteristics and its ability to operate on a single supply. Unlike most op amps running on a single supply, the inputs of the difference amplifier can be driven below 0 V. This allows the inputs of A1 to accept a negative input signal while maintaining a 0 V output. Integrated ESD diodes at the inputs provide additional robust overvoltage protection. Figure 4 shows the input and output waveform and characteristic with a 20-V p-p input signal at 1 kHz.

This improved absolute value circuit overcomes many of the limitations of the conventional rectifier design and offers unexpected value. Most remarkable is the reduced number of required components: only a single device is needed. Eliminating the external diodes also eliminates the crossover distortion. The laser-wafer-trimmed resistors are precisely matched, guaranteeing gain error of less than 0.02%. The circuit's noise gain is only 2, resulting in lower noise and lower offset and drift.

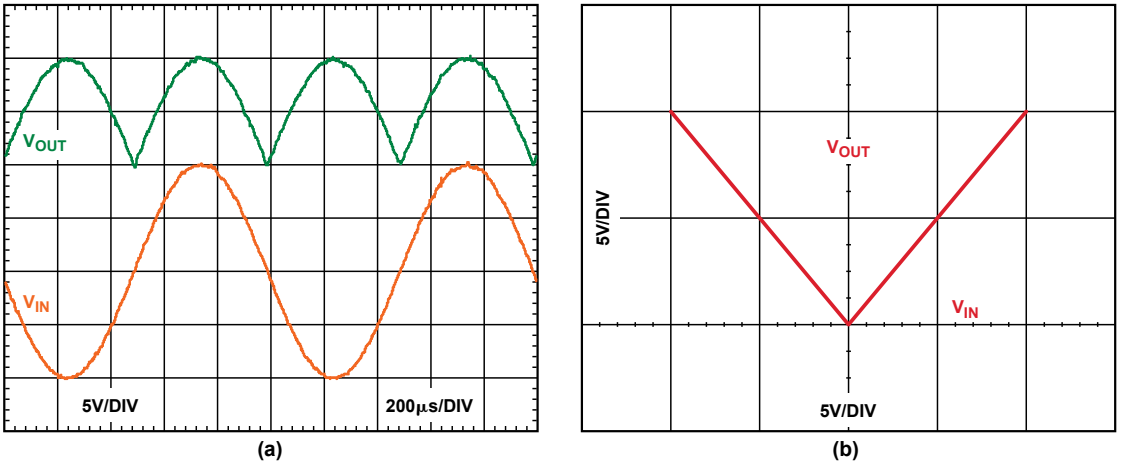

Figure 4. (a) Output and input for 20-V p-p input signal at 1 kHz. (b) Output vs. input characteristic.

Operating on a single 2-V to 36-V supply, the AD8277 consumes less than 400 µA of quiescent current.

Conclusion

A precision full-wave rectifier built with a single dual-channel difference amplifier offers several advantages over traditional designs. Notably, the need for high performance external components and dual power supplies is eliminated, drastically lowering cost and reducing complexity. The difference amplifier solution has no crossover recovery problem and is optimized for low drift over a wide temperature range. Using the AD8277, a high precision absolute value circuit can be realized at low power consumption and low cost using a single IC.

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Synchronous Inverse SEPIC Topology Provides High Efficiency for Noninverting Buck/Boost Voltage Converters

By Matthew C. Kessler

In many markets, demand is increasing for efficient noninverting dc-to-dc converters that can operate in either buck or boost mode, decreasing or increasing the input voltage to a desired regulated voltage—with minimal cost and component count. The inverse SEPIC (*single-ended primary inductor converter*), also known as the *zeta* converter, has many properties that make it ideal for this function (Figure 1). An analysis of its operation and implementation with the ADP1877 *dual-channel synchronous switching controller* will reveal its useful properties for this application.

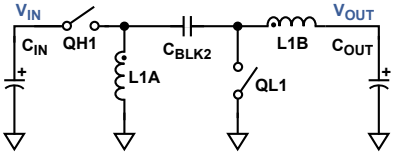

Figure 1. Inverse-SEPIC topology.

Primary switch QH1 and secondary switch QL1 operate in opposite phase from one another. During the *on* time, QH1 is conducting and QL1 is off. Current flows in two paths, as shown in Figure 2. The first is from the input, through the primary switch, the energy-transfer capacitor (C_{BLK2}), the output inductor (L1B), and the load—finally returning back to the input through ground. The second path is from the input, through the primary switch, the ground-reference inductor (L1A), and back to the input through ground.

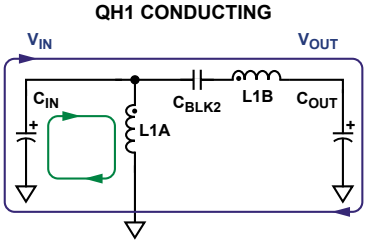

Figure 2. Current-flow diagram. QH1 is closed, QL1 is open.

During the *off* time, the switch positions are reversed. QL1 is conducting and QH1 is off. The input capacitor (C_{IN}) is disconnected, but current continues to flow through the inductors in two paths, as shown in Figure 3. The first is from the output inductor, through the load, through ground, and back to the output inductor through the secondary switch. The second path is from the ground-reference inductor, through the energy-transfer capacitor, the secondary switch, and back to the ground-reference inductor.

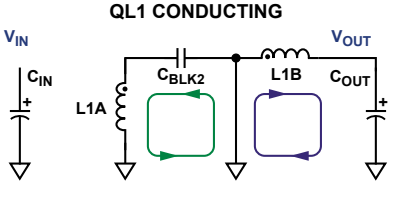

Figure 3. Energy-transfer diagram—QL1 closed and QH1 open.

Applying the principles of *inductor volt-second balance* and *capacitor charge balance*, one finds the equilibrium dc conversion ratio specified in Equation 1, where D is the converter's *duty cycle* (on time fraction of the cycle).

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D} \quad (1)$$

This suggests that if the duty cycle is greater than 0.5, a higher voltage will be regulated at the output (*boost*); if the duty cycle is less than 0.5, the regulated voltage will be lower (*buck*). Other relevant results of this analysis are that the steady-state voltage across the energy-transfer capacitor (C_{BLK2}) is equal to V_{OUT} in a lossless system; the dc value of the current through the output inductor (L1B) is equal to I_{OUT}; and the dc value of the current through the ground-reference inductor (L1A) is $I_{OUT} \times V_{OUT}/V_{IN}$. The energy-transfer capacitor also provides dc blocking from V_{IN} to V_{OUT}. This property can be attractive when there is a risk of a shorted output.

The analysis also shows that the output current in the inverse SEPIC is continuous, yielding a lower peak-to-peak output voltage ripple for a given output capacitor impedance. This allows the use of smaller, less costly output capacitors as compared to the capacitors needed to meet the same ripple requirement with discontinuous output current topologies.

Typically, the secondary switch (QL1) is a unidirectional power diode, which limits the peak efficiency of this topology. However, with a single channel of the Analog Devices ADP1877 dual-channel synchronous switching controller (see Appendix), an inverse SEPIC can be designed in a *fully synchronous configuration*, employing a bidirectional MOSFET as the secondary switch. This allows the peak efficiency to increase considerably, while at the same time decreasing the size and cost of the converter at output currents greater than 1 A.

Figure 4 shows the power stage of the fully synchronous inverse SEPIC configuration, as implemented with the ADP1877 and requiring only three small, inexpensive additional components (C_{BLK1}, D_{DRV}, and R_{DRV}) that dissipate negligible power.

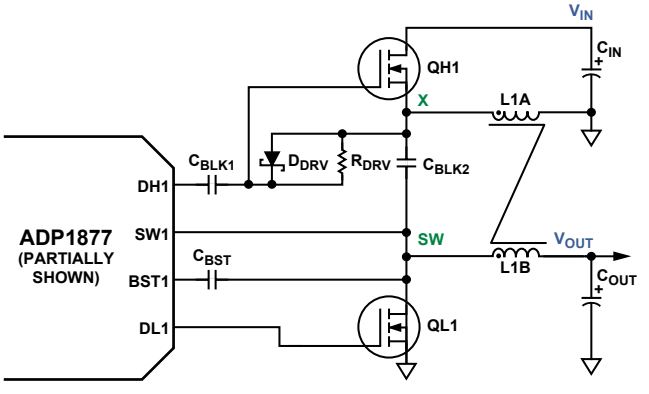

Figure 4. Power stage of a synchronous inverse SEPIC, implemented with Channel 1 of an ADP1877.

The ideal steady-state waveforms of the inverse SEPIC are shown in Figure 5. The Channel-1 switch node, SW1, (see Figure A in the Appendix) is toggled between $V_{IN} + V_{OUT}$ during the *on* time and 0 V during the *off* time. Connecting charge-pump capacitor, C_{BST}, to SW1 imposes a voltage approximately equal to $V_{IN} + V_{OUT} + 5$ V on the bootstrapped upper rail of the high-side internal driver (BST1 pin) and the output of the high-side driver (DH1 pin) during the on time, thus enhancing the primary floating N channel MOSFET switch, QH1. Clamping diode, D_{DRV}, ensures that C_{BLK1} has approximately $V_{OUT} + V_{FWD}(D_{DRV})$ across it during steady-state output, as referenced from the DH1 pin of the ADP1877 to the gate of QH1. The voltage across C_{BLK1} keeps the primary switch from developing a gate-to-source voltage that is higher than its threshold during the *off* time when the X-node voltage is approximately equal to $-V_{OUT}$.

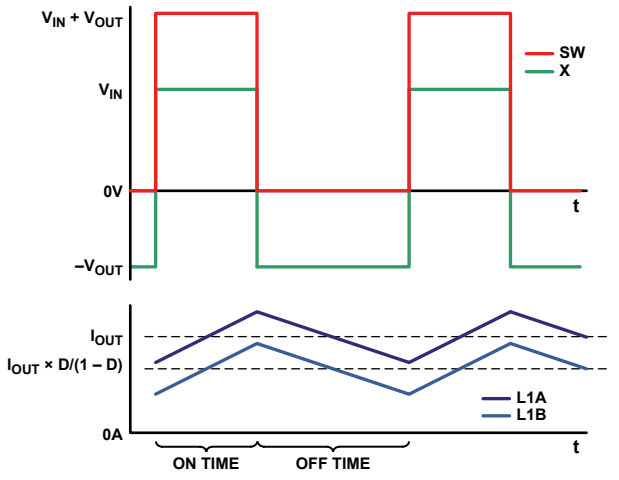

Figure 5. Ideal waveforms of synchronous inverse SEPIC (dead time ignored).

The ADP1877 has a *pulse-skip* mode that, when enabled, increases the efficiency at light loads by decreasing the switching rate, delivering just enough energy to the output to keep the output voltage in regulation—considerably decreasing the gate charge and switching loss. This mode can be enabled in both the synchronous inverse SEPIC and synchronous buck topologies. Since only a single channel of the dual-channel ADP1877 is needed for the dc-to-dc conversion circuit of Figure 4, the other channel is available for either topology.

Inductor Coupling and Energy Transfer Capacitor

In Figure 4, power inductors L1A and L1B are shown as coupled. The purpose for coupling the inductors in this topology is to reduce ripple in the output voltage and inductor current, and to increase the maximum potential closed-loop bandwidth—as will be seen in the next section.

Even though the inductors are coupled, it is undesirable for the coupling to be tight enough to transfer significant energy from one winding to the other through the core. This can be avoided by finding the leakage inductance (L_{LKG}) of the coupled inductor and sizing the energy transfer capacitor (C_{BLK2}) such that the magnitude of its complex impedance is 1/10 of the complex series impedance of the leakage inductance and the resistance (DCR) of a single winding, as designated in Equations 2, 3, and 4. Designing the circuit to conform to this relationship minimizes the energy transfer through the coupled core. The leakage inductance can be calculated from the coupling coefficient, commonly found on coupled-inductor data sheets.

$$|Z_{C_{BLK2}}| = \sqrt{ESR^2 + \left(\frac{1}{2\pi C_{BLK2} f_{SW}}\right)^2} \quad (2)$$

$$|Z_{L_{LKG}}| = \sqrt{DCR^2 + (2\pi L_{LKG} f_{SW})^2} \quad (3)$$

$$|Z_{C_{BLK2}}| \leq \frac{|Z_{L_{LKG}}|}{10} \quad (4)$$

A 1:1 turns ratio is desirable because it requires half the inductance for each winding that discrete inductors would need for a given level of output voltage ripple.[1] A ratio different from 1:1 could be used, but the results would not be accurately described by the equations in this article.

Small-Signal Analysis and Loop Compensation

A complete small-signal analysis of the inverse SEPIC converter is beyond the scope of this article; however, if one follows the following guidelines, the complete analysis becomes academic.

First, many complex impedance interactions at the resonant frequency (f_{RES}) must be calculated initially in order to find the upper limit on the target crossover frequency. When the inductors are uncoupled, this frequency decreases, significantly decreasing the potential maximum closed-loop bandwidth.

$$f_{RES} = \frac{1}{2\pi\sqrt{2L_{LKG} C_{BLK2}}} \quad (5)$$

At this frequency there can be 300° or more of "high-Q" phase lag. To avoid a low-phase-margin converter across the full load range, one should target a crossover frequency (f_{UNITY}) at 1/10 f_{RES}. Damping this resonance is largely dependent on the output loading resistance and the coupled inductor's dc resistance. To a lesser extent, damping is dependent on the *equivalent series resistance* (ESR) of the energy-transfer capacitor, and the *on* resistance of the power MOSFETs (QHl and QL1). Therefore, as the output load resistance varies, one should not be surprised to see the signature of the closed-loop transfer function change dramatically at this frequency.

The coupling coefficient is often not a well-controlled parameter, so the target crossover frequency, f_{UNITY}, should be set to a decade below f_{RES}, assuming f_{RES} is less than the switching frequency, f_{SW}. Standard "Type II" compensation—with two poles and a zero—can be used when f_{UNITY} is set appropriately.

$$f_{UNITY} = \text{Minimum}\left(\frac{f_{RES}}{10}, \frac{f_{SW}}{10}\right) \quad (6)$$

Figure 6 shows the equivalent circuit of the ADP1877's feedback loop when employed in a synchronous inverse SEPIC buck/boost topology. The upper box contains the power stage and current loop; the lower box contains the voltage feedback loop and compensation circuitry.

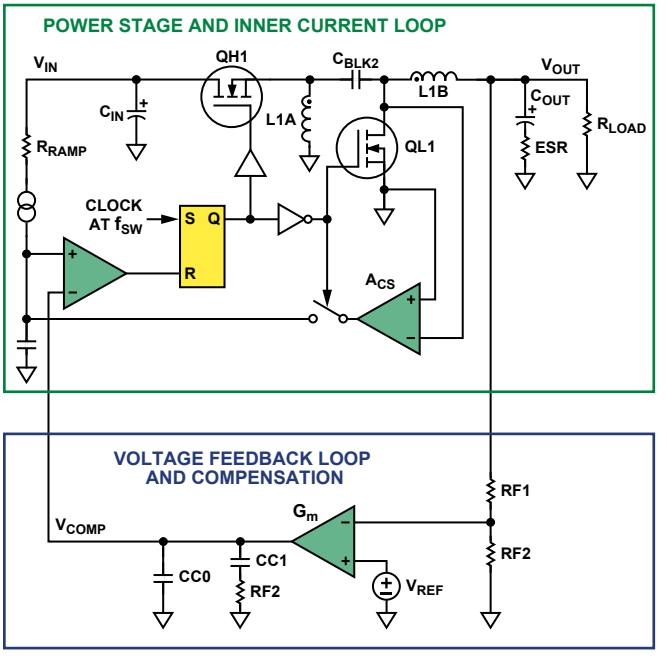

Figure 6. Power stage with inner current-sensing l-loop and compensation scheme of the ADP1877 configured in synchronous inverse SEPIC topology.

The compensation-component values in the lower box can be calculated as follows:

$$R_C = \frac{2\pi f_{UNITY} C_{OUT} (ESR + R_{LOAD})^2 V_{OUT}}{G_m G_{CS} R_{LOAD}{}^2 V_{REF}} \quad (7)$$

$$C_{C1} = \frac{C_{OUT}(R_{LOAD} + ESR)}{R_C} \quad (8)$$

$$C_{C0} = \frac{C_{C1} ESR}{R_{LOAD}} \quad (9)$$

G_{CS}, the transconductance of the converter, is calculated by:

$$G_{CS} = \frac{1}{A_{CS} R_{DS(ON)\text{MIN}} \left(1 + \frac{D}{1-D}\right)} = \frac{1}{A_{CS} R_{DS(ON)\text{MIN}} \left(\frac{1}{1-D}\right)} = \frac{\Delta I_{OUT}}{\Delta V_{COMP}} \quad (10)$$

C_{OUT} is the output capacitance of the converter. ESR is the equivalent series resistance of the output capacitor. R_{LOAD} is the minimum output load resistance. A_{CS} is the current-sense gain, which, with the ADP1877, is selectable in discrete steps from 3 V/V to 24 V/V. G_m is the transconductance of the error amplifier, 550 µs for the ADP1877. V_{REF} is the reference voltage that is tied to the positive input of the error amplifier, 0.6 V for the ADP1877.

G_{CS} is a frequency-independent gain term that varies with $R_{DS(ON)}$, the resistance of the secondary switch when enhanced. It is expected that the highest crossover frequency occurs when this resistance and the duty cycle, D, are at their lowest.

To ensure that the compensation clamp voltage is not reached at maximum output current, the highest value of current-sense gain (A_{CS}) that obeys the following inequality should be selected:

$$2.25\text{ V} \geq A_{CS} R_{DS(ON)MAX} \left(I_{OUT}\left(\frac{1}{1-D}\right) - \frac{\Delta I_L}{1.2}\right) + 0.75\text{ V} \quad (11)$$

where ΔI_L is the peak-to-peak inductor ripple current.

$$I_L = \frac{V_{IN} D}{2 L_{1B} f_{SW}} \quad (12)$$

If excessive slope compensation is added, the equations in this section will be less accurate: the dc gain will decrease and the dominant pole location—due to the output filter—will increase in frequency.

Slope Compensation

For synchronous inverse SEPICs implemented with the ADP1877, the subharmonic oscillation phenomenon in current-mode controllers[2] must be taken into account.

By setting R_{RAMP} according to the following equation, the quality factor of the sampling poles can be set to unity, which prevents subharmonic oscillations,[3] assuming f_{UNITY} was set appropriately.

$$R_{RAMP} = \frac{(V_{IN\,\text{MIN}} - 0.2) L_1 (1-D)}{5 A_{CS} R_{DS(ON)\,\text{MAX}} \times 6\text{ pF} \times V_{IN\,\text{MIN}} \left(\frac{1}{\pi} + 0.5\right)} \quad (13)$$

It is noteworthy that as $R_{DS(ON)}$—the resistance of the secondary switch when enhanced—decreases, the Q of the sampling poles also decreases. If this, in conjunction with other related tolerances, results in a Q of less than 0.25, one should perform a simulation to ensure the converter does not have excessive slope compensation and is not "too voltage mode" with tolerance considered. The value of R_{RAMP} must result in a current between 6 µA and 200 µA into the ADP1877's RAMP pin, as calculated with Equation 14.

$$I_{RAMP} = \frac{V_{IN} - 0.2}{R_{RAMP}} \quad (14)$$

Power Component Stresses

From the current-flow diagrams in Figure 2 and Figure 3, one can see that the power MOSFETs, when conducting, carry the sum of the inductor currents. Accordingly, the dc component of the current through both switches is

$$I_{DC} = I_{OUT}\left(1 + \frac{D}{1-D}\right) = I_{OUT}\frac{1}{1-D} \quad (15)$$

If the coupling ratio of the inductors is 1:1, the ac component of the current through both switches is

$$I_{AC} = \frac{V_{IN} D}{L_{1A} f_{SW}} \quad (16)$$

With these values known, one can quickly calculate the rms values of the current through each switch. In conjunction with the $R_{DS(ON)MAX}$ of the selected MOSFETs, these can be used to ensure that the MOSFETs are thermally stable, with power dissipation low enough to meet the efficiency requirements.

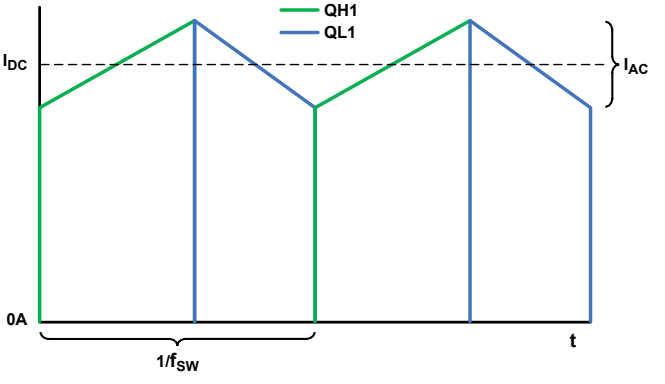

Figure 7. Ideal current waveforms of synchronous inverse SEPIC (dead time ignored).

Calculating switching loss in the primary switch accurately is beyond the scope of this article, but it should be noted that, in transitioning from high-resistance- to low-resistance states, the voltage across the MOSFET will swing from ~V_{IN} + V_{OUT} to ~0 V, and the current through the device will swing from 0 A to $I_{OUT}[1/(1 - D)]$. Switching loss can be the predominant loss with swings of these magnitudes, a factor one should be aware of when picking a MOSFET for which the reverse transfer capacitance (C_{RSS}) and $R_{DS(ON)}$ are inversely proportional.

The *drain-source breakdown voltage* (BV_{DSS}), for both the primary and secondary switches, must be greater than the input voltage plus the output voltage (see Figure 5).

The peak-to-peak output-voltage ripple (ΔV_{RIPPLE}) is approximated by

$$\Delta V_{RIPPLE} \approx \frac{\Delta I_L}{8 f_{SW} C_{OUT}} + \Delta I_L \times ESR \quad (17)$$

Table 1. Power Components

Designator	Part Number	Manufacturer	Value	Package	Comment
QH1/QL1	FDS6572A	Fairchild Semiconductor	20 BV_{DSS}	SO8	Power MOSFET/6 mΩ (max) @ 4.5 Vgs @ 25°C Tj
L1A/B	PCA20EFD-U10S002	TDK	3.4 µH per winding	30 mm × 22 mm × 12 mm	1:1:1:1:1:1 coupled inductor/ferrite/35.8 mΩ (max) DCR per winding

The rms value of the current through the output capacitor ($I\,rms\,C_{OUT}$) is

$$I\,rms\,C_{OUT} \approx \frac{\Delta I_L}{2\sqrt{3}} \quad (18)$$

The peak-to-peak inductor current (ΔI_L) designated in Equation 12 depends on the input voltage, so one must ensure that, as this parameter varies, the output-voltage ripple does not exceed the specification and the rms current through the output capacitor does not exceed its rating.

For synchronous inverse SEPICs implemented with the ADP1877, the input voltage plus the output voltage must not exceed 14.5 V because the charge-pump capacitor is connected to the switch node, which reaches $V_{IN} + V_{OUT}$ when the primary switch is conducting.

Lab Results

Figure 8 shows the efficiency of the synchronous inverse SEPIC as a function of load current for 5-V output with 3-V and 5.5-V inputs—a common situation for applications that need to toggle between 3.3 V and 5.0 V input rails, or when the input voltage is margined on-the-fly to optimize for system efficiency. With 1-A to 2-A loads, and the input voltage both above and below the output voltage, the efficiency of the converter reaches over 90%.

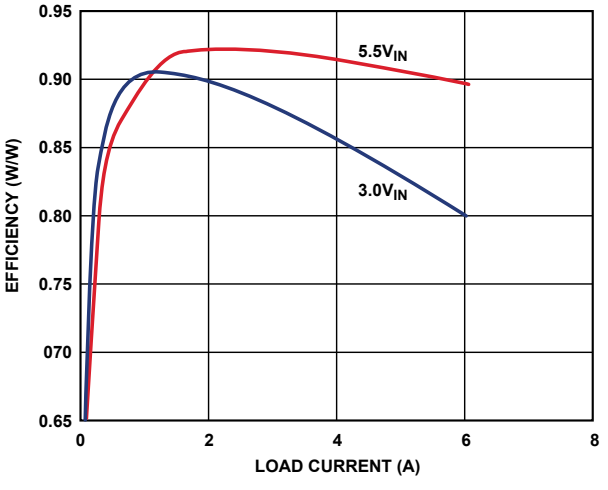

Figure 8. Efficiency vs. load current.

The bill of materials for the relevant power components associated with Figure 8 is seen in Table 1; it includes only common off-the-shelf components. A comparable asynchronous design using an industry-leading Schottky diode with a low forward-voltage drop in place of QL1 is almost 10% less efficient at full load at both input voltages. The asynchronous design would also be larger and more expensive and would be likely to require a costly heat sink.

Conclusion

The need for high efficiency noninverting converters that provide both higher and lower voltages than the input (boost and buck) is increasing in many markets. The Analog Devices ADP1877 dual-channel synchronous switching controller allows the high-loss power diode commonly used in the power stage to be replaced by a low-loss MOSFET. This increase in efficiency can reduce cost and circuit footprint—and allow the system to meet stringent energy requirements. Component values for robust compensation can be quickly calculated by following a few guidelines, and high efficiency can be achieved with common off-the-shelf components.

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Author

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Appendix

The ADP1877, shown in Figure A, is a Flex-Mode™ (proprietary architecture of Analog Devices, Inc.) dual-channel, switching controller with integrated drivers that drive N-channel synchronous power MOSFETs. The two PWM outputs are phase-shifted by 180°, which reduces the input rms current, thus minimizing required input capacitance.

The boost diodes are built into the ADP1877, thus lowering the overall component count and system cost. The ADP1877 can be set to operate in pulse-skip high-efficiency mode under light load, or in PWM continuous conduction mode.

The ADP1877 includes externally adjustable soft start, output overvoltage protection, externally adjustable current limit, power good, and a programmable oscillator frequency that ranges from 200 kHz to 1.5 MHz. The ADP1877 provides an output voltage accuracy of ±0.85% from –40°C to +85°C and ±1.5% from –40°C to +125°C junction temperature. Powered by a 2.75-V to 14.5-V supply, it is available in a 32-lead, 5 mm × 5 mm LFCSP package.

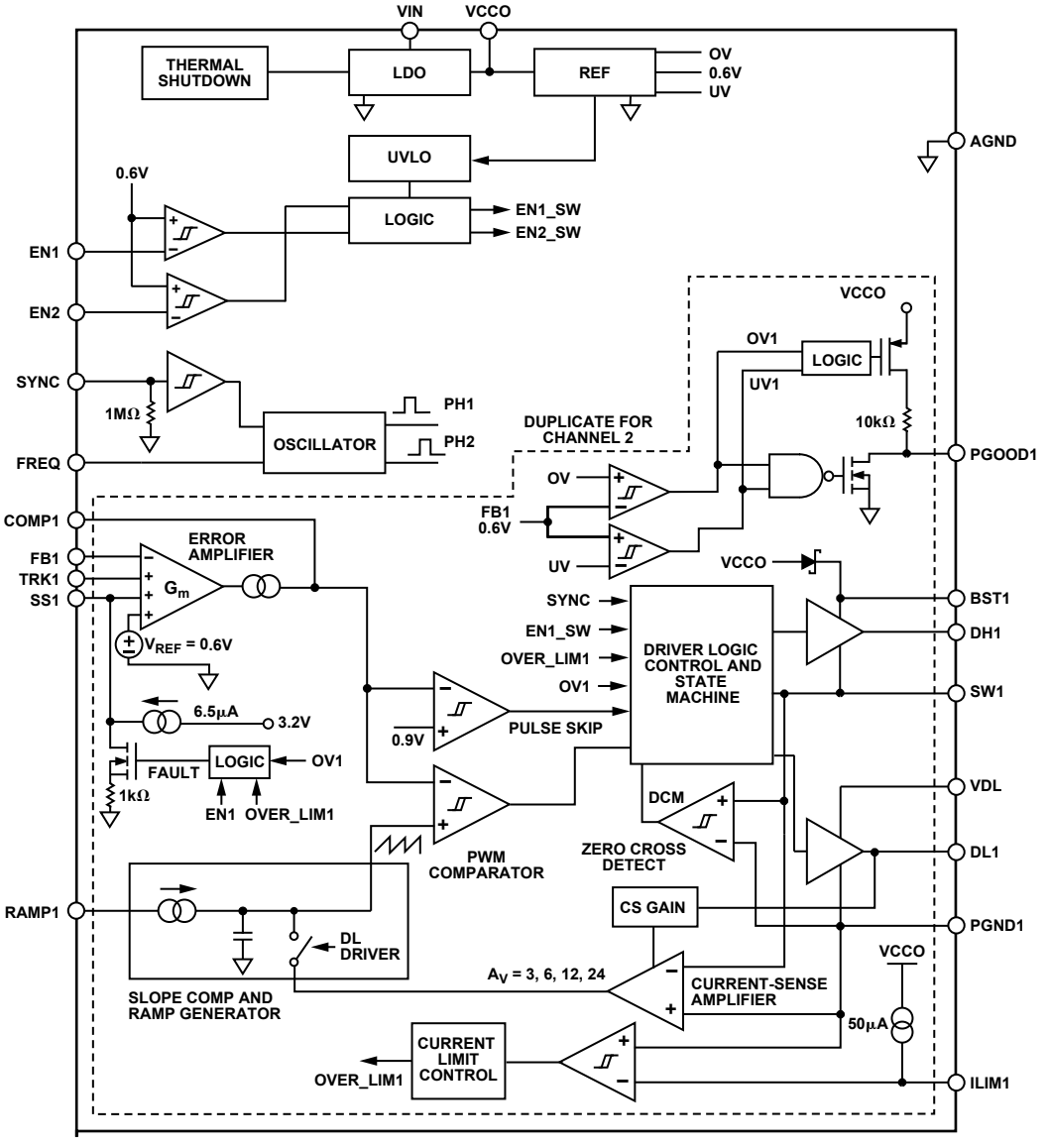

Figure A. ADP1877 simplified block diagram. Only Channel 1 is shown; Channel 2 is identical, with suffixes “2.”

Ultralow Distortion Audio Panpot Amplifier

By Chau Tran

An audio "panpot" circuit, shown in Figure 1, continuously varies the position of a monophonic audio signal between left and right stereo channels in response to a potentiometer setting. Low cost and low distortion are important considerations for audio circuits. The AD8273[1] dual low-distortion difference amplifier uses internal gain setting resistors to ensure excellent matching between the two channels. With no external components, each channel is configured as two high-performance amplifiers with a gain of 3. In the audio frequency range, the total harmonic distortion is less than 0.0007%.

Although this circuit can be built discretely, integrating the amplifiers and resistors on a single chip offers advantages to board designers, including improved specifications, less PCB area, and lower production cost.

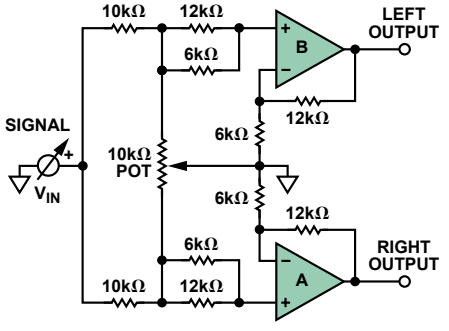

Figure 1. Audio panpot amplifier.

In this circuit, the signal is split between the two amplifiers, using series 10-kΩ resistors. A potentiometer, with a grounded wiper, is inserted between the two noninverting inputs. The combination of the potentiometer and the 10 kΩ resistors presents a light load that can be easily driven by most sources. The amplifiers are configured for a gain of 3. When the potentiometer wiper is at either end, one input is grounded, so no signal gets through to the corresponding output. The other input sees $V_{IN}/2$, so its output is $1.5 \times V_{IN}$. With the wiper in the middle, the input to both amplifiers is $V_{IN}/3$, so the output of each amplifier is V_{IN}. Thus, by moving the wiper (either mechanically or electronically), the signal level varies continuously from 0 to $1.5 \times V_{IN}$ on one channel and from $1.5 \times V_{IN}$ to 0 on the other channel, so that, to a listener, the source appears to move across the sound stage from one channel to the other. This allows the image, or the apparent source of the sound, to be placed at any location between the left and right speakers.

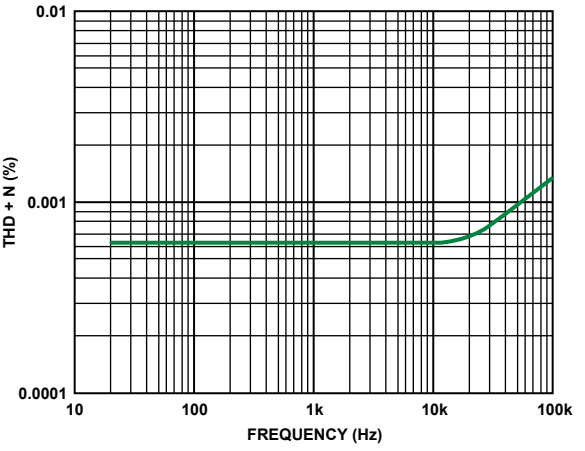

Figure 2. Total harmonic distortion and noise vs. frequency.

Figure 2 shows the total harmonic distortion and noise over the audio frequency range. The error increases with frequency, but the total error is still less than 0.0007% at 20 kHz. Figure 3 shows the connections to the IC.

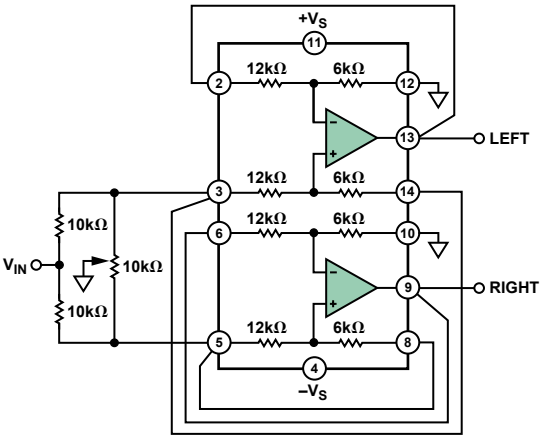

Figure 3. Connection diagram.

References

[1] www.analog.com/en/audiovideo-products/audio-amplifiers/ad8273/products/product.html.

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Differential-Output Difference Amplifier System with G = ½

By Moshe Gerstenhaber and Michael O'Sullivan

Designed on small-geometry processes, high-performance ADCs typically run on a single 1.8-V to 5-V supply or dual ±5-V supplies. To process real-world signals of ±10 V or larger, the ADC is often preceded by an amplifier that attenuates the signal to keep it from saturating or damaging the ADC inputs. These amplifiers usually have single-ended outputs, but differential outputs would be preferable to capture the full benefits of the differential-input ADC, including increased dynamic range, improved common-mode rejection, and reduced noise sensitivity. Figure 1 shows a differential-output amplifier system with gain of ½.

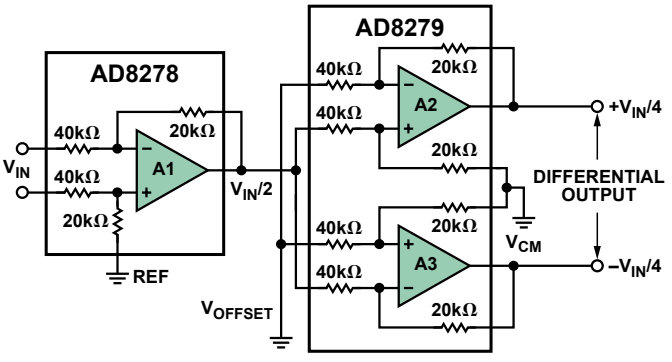

Figure 1. Functional block diagram of differential-output difference amplifier with G = ½.

Differential amplifier A1 is configured for a gain of ½. The output of this amplifier is fed into the noninverting input of amplifier A2 and the inverting input of amplifier A3. Amplifiers A2 and A3 also operate at a gain of ½. Their outputs, 180 degrees out of phase, form a differential output. The differential output voltage, $V_{OUT}A2 - V_{OUT}A3$, is equal to $V_{IN}/4 - (-V_{IN}/4)$, or a total differential output voltage of $V_{IN}/2$, as desired.

The V_{OFFSET} terminal can be used to offset the output and increase the dynamic range of the ADC. The differential gain from V_{OFFSET} to the output is –1. Connect this node to ground if offset adjustment is not required.

The V_{CM} terminal sets the common-mode voltage of the differential output. This is particularly useful when driving single-supply ADCs, as the common-mode output of the circuit can be set to midsupply. The gain from V_{CM} to the output is 1. Connect this node to ground if common-mode adjustment is not required.

Figure 2 demonstrates the circuit's performance. The input is a 25-kHz, 20-V p-p sine wave. Channel 1 is the noninverting output; Channel 2 is the inverting output; Channel 3 is the input. The Math Channel is the difference between the two outputs. Each output is ¼ of the input signal; the two outputs are inverted with respect to each other; and their difference is ½ of the input signal.

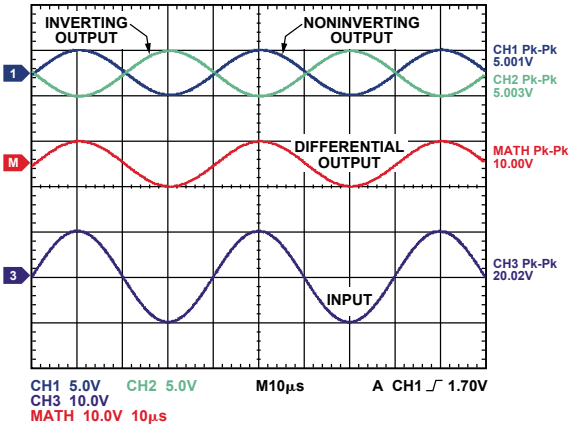

Figure 2. Differential output is ½ of the input signal.

Figure 3 shows the gain vs. frequency response of the circuit, demonstrating that it is stable, with less than 1-dB peaking over a 1-MHz bandwidth.

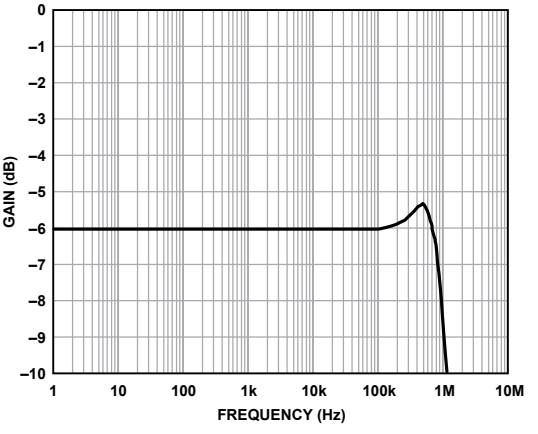

Figure 3. Frequency response of differential-output difference amplifier.

Figure 4 demonstrates that the circuit's response to large square-wave inputs has no appreciable overshoot and a quick settling time. The differential output slews twice as fast as the individual outputs because each amplifier carries only half of the signal.

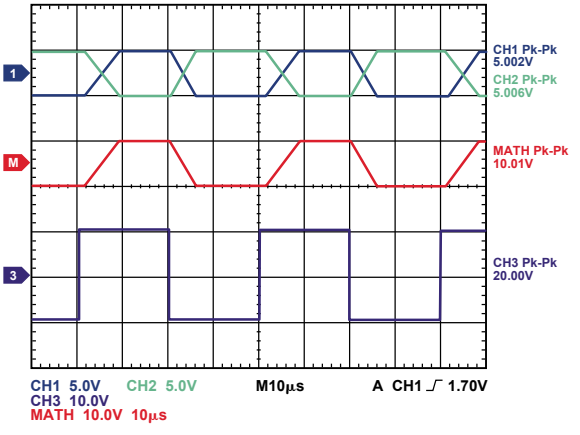

Figure 4. Large-signal performance of the differential-output difference amplifier.

The AD8279[1] dual difference amplifier is available in a narrow-body 14-lead SOIC package. The AD8278[2] is available in an 8-lead MSOP package. Because the precision laser-trimmed resistors are integrated onto the same chip as the amplifiers, their offset, gain, common-mode errors—and drift over temperature—are minimized, making for a high-precision system. Despite the low power consumption of the AD8278 (200 μA) and AD8279 (200 μA per amplifier), the system has a 1-MHz bandwidth and a 2.4-V/μs slew rate. The AD8278 and AD8279 can operate over a very large supply voltage range, from a single 2.5-V supply to dual ±18-V supplies. The inputs can swing well beyond the supply rails, enabling them to measure large signals (±20 V or more) in the presence of large common-mode voltages and noise, making this an ideal front end for high-performance, low-voltage ADCs.

References

[1] www.analog.com/en/amplifiers-and-comparators/difference-amplifiers/ad8279/products/product.html.

[2] www.analog.com/en/amplifiers-and-comparators/difference-amplifiers/ad8278/products/product.html.

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Full-Featured Pedometer Design Realized with 3-Axis Digital Accelerometer

By Neil Zhao

Introduction

Pedometers, now popular as an everyday exercise progress monitor and motivator, can encourage individuals to compete with themselves in getting fit and losing weight. Early designs used a weighted mechanical switch to detect steps, plus a simple counter. When these devices are shaken, one can hear a metal ball sliding back and forth, or a pendulum striking stops as it swings.

Today, advanced pedometers rely on *microelectromechanical systems* (MEMS) inertial sensors and sophisticated software to detect true steps with high probability; MEMS inertial sensors permit more accurate detection of steps and fewer false positives. Taking advantage of the low cost and minimal space- and power requirements of MEMS inertial sensors, pedometers are being integrated into an increasing number of portable consumer electronic devices—such as music players and mobile phones. The small, thin, low-power ADXL335, ADXL345, and ADXL346 3-axis accelerometers from Analog Devices are very suitable for such applications.

This article, based on a study of the characteristics of each step a person takes, describes a reference design using the 3-axis ADXL345 accelerometer in a full-featured pedometer that can recognize and count *steps*, as well as measure *distance*, *speed*, and—to an extent—*calories* burned.

The ADXL345's proprietary (patent pending), on-chip, 32-level first-in, first-out (FIFO) buffer can store data and operate on it for pedometer applications to minimize host processor intervention, thus saving system power—a big concern for portable devices. Its 13-bit resolution (4 m*g*/LSB) allows pedometers to even measure low-speed walking (where each step represents about 55 m*g* of acceleration change) with reasonable accuracy.

Understanding the Model

From the characteristics that can be used to analyze running or walking, we choose *acceleration* as the relevant parameter. The three components of motion for an individual (and their related axes) are forward (*roll*), vertical (*yaw*), and side (*pitch*), as shown in Figure 1. The ADXL345 senses acceleration along its three axes: *x*, *y*, and *z*. The pedometer will be in an unknown orientation, so the measurement accuracy should not depend critically on the relationship between the motion axes and the accelerometer's measurement axes.

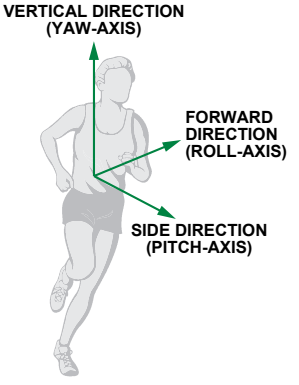

Figure 1. Definition of each axis.

Let's think about the nature of walking. Figure 2 depicts a single step, defined as a unit cycle of walking behavior, showing the relationship between each stage of the walking cycle and the change in vertical and forward acceleration.

Figure 3 shows a typical pattern of x-, y-, and z measurements corresponding to vertical, forward, and side acceleration of a running person. At least one axis will have relatively large periodic acceleration changes, no matter how the pedometer is worn, so peak detection and a dynamic threshold-decision algorithm for acceleration on all three axes are essential for detecting a unit cycle of walking or running.

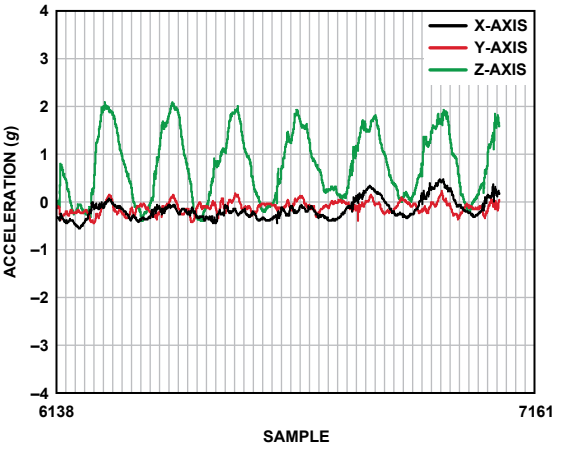

Figure 3. Typical pattern of *x*-, *y*-, and *z* accelerations measured on a running individual.

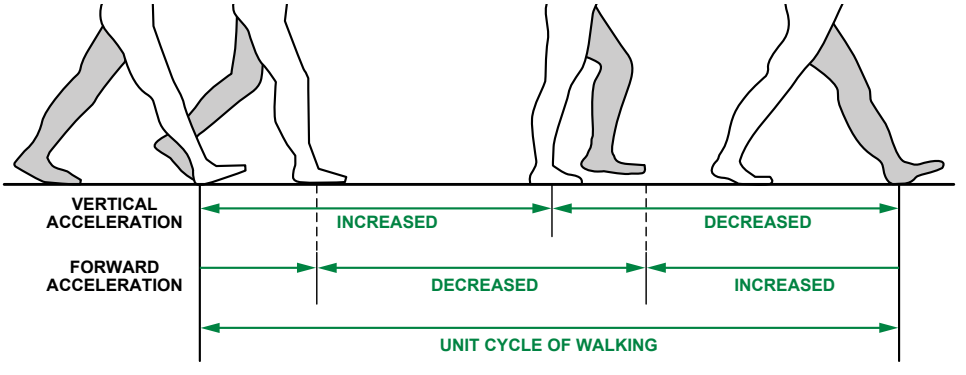

Figure 2. Walking stages and acceleration pattern.

Algorithm

Steps Parameter

Digital Filter: First, a digital filter is needed to smooth the signals shown in Figure 3. Four registers and a summing unit can be used, as shown in Figure 4. Of course, more registers could be used to make the acceleration data smoother, but the response time would be slower.

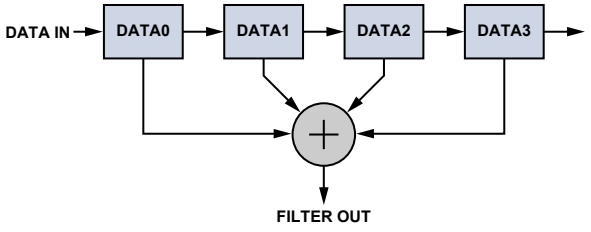

Figure 4. Digital filter.

Figure 5 demonstrates the filtered data from the most active axis of a pedometer worn by a walking person. The peak-to-peak value would be higher for a runner.

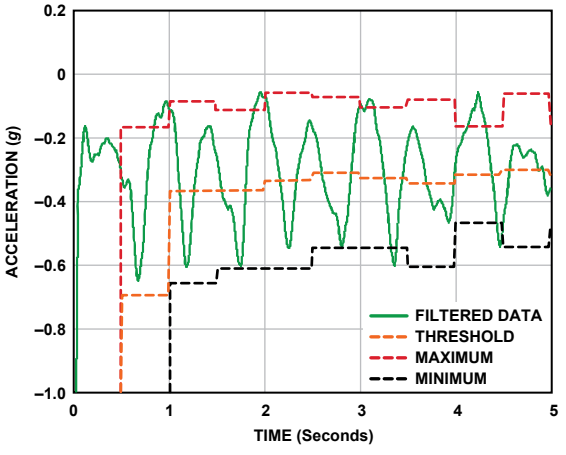

Figure 5. Filtered data of the most active axis.

Dynamic Threshold and Dynamic Precision: The system continuously updates the maximum and minimum values of the 3-axis acceleration every 50 samples. The average value, (*Max* + *Min*)/2, is called the *dynamic threshold level*. For the following 50 samples, this threshold level is used to decide whether steps have been taken. As it is updated every 50 samples, the threshold is *dynamic*. This choice is adaptive and fast enough. In addition to dynamic threshold, dynamic precision is also used for further filtering as shown in Figure 6.

A linear-shift-register and the dynamic threshold are used to decide whether an effective step has been taken. The linear-shift-register contains two registers, a sample_new register and a sample_old register. The data in these are called *sample_new* and *sample_old*, respectively. When a new data sample comes, *sample_new* is shifted to the sample_old register unconditionally. However, whether the *sample_result* will be shifted into the sample_new register depends on a condition: If the changes in acceleration are greater than a predefined precision, the newest sample result, *sample_result*, is shifted to the sample_new register; otherwise the sample_new register will remain unchanged. The shift register group can thus remove the high-frequency noise and make the decision more precise.

A *step* is defined as happening if there is a negative slope of the acceleration plot (*sample_new* < *sample_old*) when the acceleration curve crosses below the dynamic threshold.

Peak Detection: The step counter calculates the steps from the *x*-axis, *y*-axis, or *z*-axis, depending on which axis's acceleration change is the largest one. If the changes in acceleration are too small, the step counter will discard them.

The step counter can work well by using this algorithm, but sometimes it seems too sensitive. When the pedometer vibrates very rapidly or very slowly from a cause other than walking or running, the step counter will also take it as a step. Such invalid vibrations must be discarded in order to find the true rhythmic steps. *Time window* and *count regulation* are used to solve this problem.

Time window is used to discard the invalid vibrations. We assume that people can run as rapidly as five steps per second and walk as slowly as one step every two seconds. Thus, the interval between two valid steps is defined as being in the time window [0.2 s to 2.0 s]; all steps with intervals outside the time window should be discarded.

The ADXL345's feature of user-selectable output data rate is helpful in implementing the time window. Table 1 shows the configurable data rate (and current consumption) at T_A = 25°C, V_S = 2.5 V, and $V_{DD\ I/O}$ = 1.8 V.

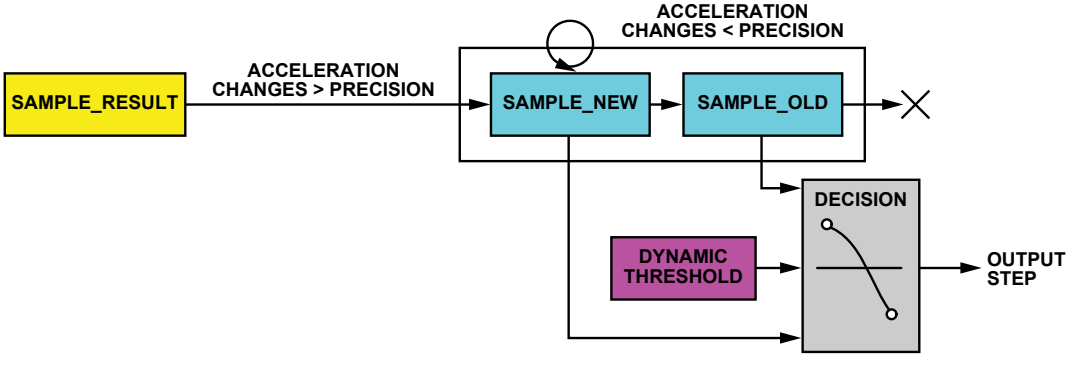

Figure 6. Dynamic threshold and dynamic precision.

Table 1. Data Rate and Current Consumption

Output Data Rate (Hz)	Bandwidth (Hz)	Rate Code	I_{DD} (μA)
3200	1600	1111	145
1600	800	1110	100
800	400	1101	145
400	200	1100	145
200	100	1011	145
100	50	1010	145
50	25	1001	100
25	12.5	1000	65
12.5	6.25	0111	55
6.25	3.125	0110	40

This algorithm uses a 50-Hz data rate (20 ms). A register named *interval* records how many times the data have updated during the two steps. If the value of interval is between 10 and 100, it means that the time between two steps is in the valid window; otherwise, the interval is outside the time window and the step is invalid.

Count regulation determines whether steps are part of a rhythmic pattern. The step counter has two working states: searching regulation and found out regulation. When the step counter starts working, it works in searching regulation mode. Suppose that *in regulation* exists after four continuous valid steps. Then the result is refreshed and displayed, and the step counter will work in found out regulation mode. Working in this mode, the step count would be refreshed after every valid step. But if even one invalid step is found, the step counter will return to searching regulation mode and search for four continuous valid steps.

Figure 7 shows the algorithm flowchart for the steps parameter.

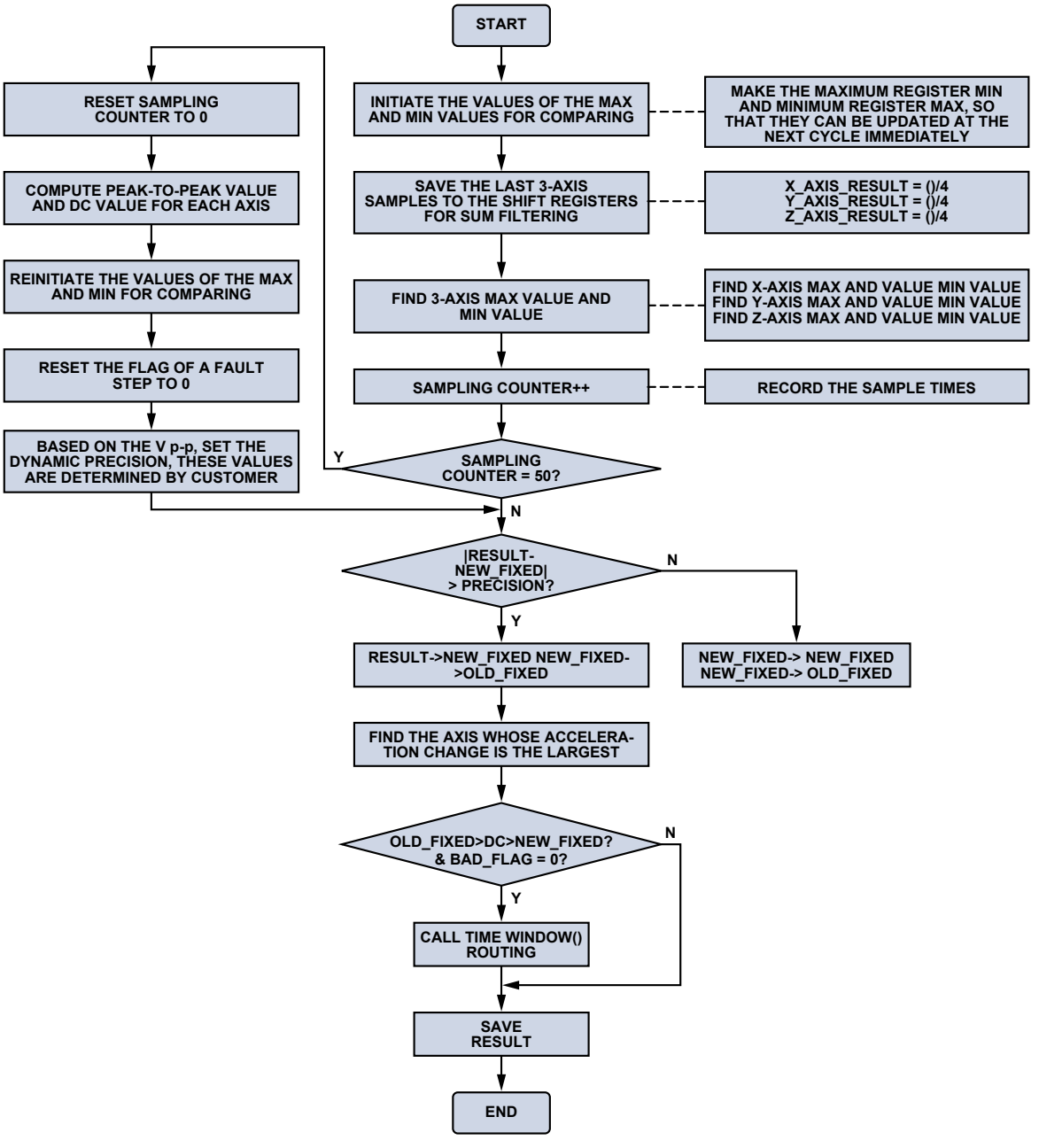

Figure 7. Steps parameter algorithm flowchart.

Distance Parameter

After computing the steps parameter according to the algorithm above, we can use Equation 1 to get the distance parameter.

$$Distance = number\ of\ steps \times distance\ per\ step \quad (1)$$

Distance per step depends on the speed and the height of user. The step length would be longer if the user is taller or running at higher speed. The reference design updates the distance, speed, and calories parameter every two seconds. So, we use the steps counted in every two seconds to judge the current stride length. Table 2 shows the experimental data used to judge the current stride.

Table 2. Stride as a Function of Speed (steps per 2 s) and Height

Steps per 2 s	Stride (m/s)
0~2	Height/5
2~3	Height/4
3~4	Height/3
4~5	Height/2
5~6	Height/1.2
6~8	Height
>=8	1.2 × Height

An interval of 2 s can be calculated accurately from the number of samples. Referring to the 50-Hz data rate, the processor can send the corresponding command to the PC every 100 samples. The processor uses a variable named *m_nLastPedometer* to record the step count at the beginning of every 2-s interval and a variable named *m_nPedometerValue* to record the step count at the end of every 2-s interval. Then the steps per 2 s is calculated by *m_nPedometerValue* minus *m_nLastPedometer*.

Although the data rate is 50 Hz, the ADXL345's on-chip FIFO makes it unnecessary for the processor to read the data every 20 ms, minimizing the burden on the host processor. The buffer has four modes: *bypass*, *FIFO*, *stream*, and *trigger*. In FIFO mode, data from measurements of the *x*-, *y*-, and *z*-axes are stored in FIFO. When the number of samples in FIFO equals the level specified in the samples bits of the FIFO_CTL register, the watermark interrupt is set. As previously discussed, people can run as fast as five steps per second, so the result should be refreshed every 0.2 s to show the real-time result. The processor only needs to fetch data from the ADXL345 every 0.2 s; it can be awakened by *watermark interrupt*. The other functions of the FIFO are also very useful. Using *trigger* mode, the FIFO can let us know what happens before the interrupt. Since the proposed solution does not use the other FIFO functions, they will not be discussed any further.

Speed Parameter

Speed = *distance*/*time*, so Equation 2 can be used to get the speed parameter, as steps per 2 s and stride have all been calculated according to the algorithm above.

$$Speed = steps\ per\ 2\ s \times stride/2\ s \quad (2)$$

Calories Parameter

There is no accurate means for calculating the rate of expending calories. Some factors that determine it include body weight, intensity of workout, conditioning level, and metabolism. We can estimate it using a conventional approximation, however. Table 3 shows a typical relationship between calorie expenditure and running speed.

Table 3. Calories Expended vs. Running Speed

Running Speed (km/h)	Calories Expended (C/kg/h)
8	10
12	15
16	20
20	25

From Table 3, we can get (3).

$$Calories\ (C/kg/h) = 1.25 \times running\ speed\ (km/h) \quad (3)$$

The unit of the speed parameter used above is m/s; converting km/h to m/s gives Equation 4.

$$\begin{aligned} Calories\ (C/kg/h) &= 1.25 \times speed\ (m/s) \times 3600/1000 \\ &= 4.5 \times speed\ (m/s) \end{aligned} \quad (4)$$

The calories parameter would be updated every two seconds with the distance and speed parameters. So, to account for a given athlete's weight, we can convert Equation 4 to Equation 5 as indicated. Weight (kg) is a user input, and one hour is equal to 1800 two-second intervals.

$$\begin{aligned} Calories\ (C/2\ s) &= 4.5 \times speed \times weight/1800 \\ &= speed \times weight/400 \end{aligned} \quad (5)$$

If the user takes a break in place after walking or running, there would be no change in steps and distance, speed should be zero, then the calories expended can use Equation 6 since the caloric expenditure is around 1 C/kg/hour while resting.

$$Calories\ (C/2\ s) = 1 \times weight/1800 \quad (6)$$

Finally, we can add calories for all two-second intervals together to get the total calories expended.

Hardware Connection

The ADXL345 is easy to connect to any processor using I²C® or SPI digital communications protocols. Figure 8 shows a simplified schematic of the demonstration equipment, which is powered by 3-V batteries. The /CS pin of the ADXL345 is tied to V_S on the board to choose I²C mode. A low-cost, precision analog microcontroller, the ADuC7024, is used to read data from the ADXL345, implement the algorithm, and send the result to the PC via a UART. SDA and SCL, the data and clock for I²C bus, are connected from the ADXL345 to the corresponding pins of ADuC7024. Two interrupt pins of the ADXL345 are connected to IRQ inputs of ADuC7024 to generate various interrupt signals and wake up the processor.

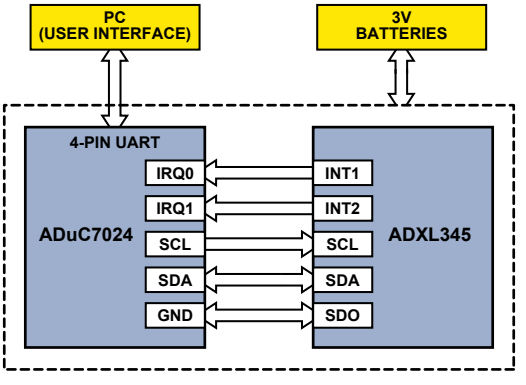

Figure 8. Simplified schematic of hardware system.

User Interface

The user interface displays the test data and responds to commands from the operator. The serial port should be opened and communications links should be started after the user interface (UI) is running. The demo can then run continuously. Figure 9 shows the test demo when the user is walking or running with the pedometer. Users can input their own height and weight data. Distance, speed, and calorie parameters will be calculated based on these data.

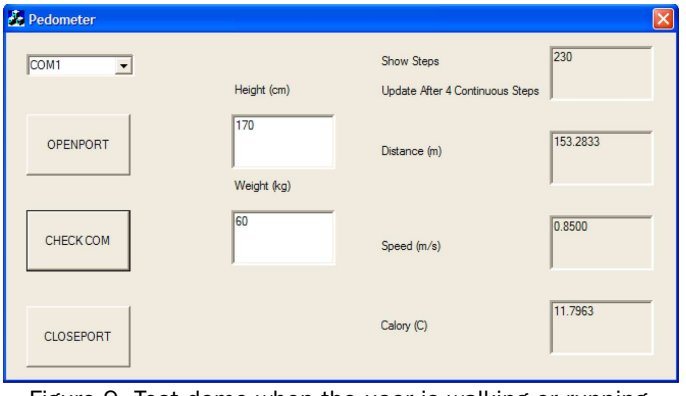

Figure 9. Test demo when the user is walking or running with the pedometer.

Conclusion

The ADXL345 is an excellent accelerometer for pedometer applications. Taking advantage of its small, thin, 3-mm × 5-mm × 0.95-mm plastic package, pedometers using it can be found in medical instruments, as well as fancy consumer electronic devices. Its low 40-μA power requirement in measurement mode and 0.1 μA in standby mode make it an ideal choice for battery-powered products. Substantial savings in power result from the embedded FIFO, which minimizes the host processor's load. Also, the selectable output data rate can be used to save a timer in the processor. The 13-bit resolution makes it possible for small peak-to-peak changes to be detected, leading to the possibility of high-accuracy pedometers. Finally, combining the 3-axis output feature and the algorithm described above, users can wear the pedometer in just about any location and position.

A couple of further ideas: If the application is extremely cost-sensitive, or if an analog-output accelerometer is preferred, the ADXL335—a small, thin, low power, complete 3-axis accelerometer with signal-conditioned voltage output—is recommended. If PCB size is of critical importance, the ADXL346 is recommended. This low-power device, with even more built-in features than the ADXL345, is supplied in a small, thin, 3-mm × 3-mm × 0.95-mm plastic package. Its supply voltage range is 1.7 V to 2.75 V.

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References

1. Data sheets and additional product information on all Analog Devices products can be found at www.analog.com.
2. www.analog.com/en/mems/low-g-accelerometers/products/index.html.

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