Amplifiers | Power Management | Processors | DSP | RF | MEMS | Converters

Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

Volume 39, Number 4, 2005

In This Issue

ANALOG DEVICES

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Editors' Notes

40TH ANNIVERSARIES

We're winding down the celebration of the 40th anniversary of Analog Devices, Inc., but inspection of your calendar will confirm that—by the time you receive these printed pages—*Analog Dialogue* will be launched well into its 40th year of existence (and eighth year live online). As a final reminder of ADI's 40th, if you're interested in the high points of our corporate history, the spread on pages 10-11 of the last issue, Volume 39, Number 3, depicts the contents page of a timeline accessible on the Web (www.analog.com/timeline); in it you can click on any year to access a brief audiovisual clip reviewing some of that year's major corporate events.

This publication has served its several generations of readers well—offering in-depth articles on design, technology, and applications of ADI's many innovative products, brief introductions to hundreds of significant new products, and a growing *potpourri* of links to useful information of all kinds, from data-sheet revisions, book reviews, application notes, and patent grants to articles in the trade press.

Interestingly, the arrival of the company's 40th anniversary showed us an unheralded additional value of *Analog Dialogue*: its usefulness to *us* as a cumulative *history* of our products and technologies—a fount of information for nurturing the retrospective activities of the celebration (for example, the above-mentioned timeline). Although it also reminded us of the occasional lost opportunity and no-go setback, it is a remarkable chronicle of progress. In the coming year, part of our celebration will be to share the early parts of the story with those of you who were too young to experience it and to refresh the memory of those who enjoy nostalgia.

THE QUESTION OF ANALOG

In this growingly "digital" age, the lay world has increasingly come to believe that "analog is antique." We sometimes are asked, "When are you going to change your name to something more modern?" In actuality, everything we make is an *analog device*; analog is the tangible world of time, space, matter, and energy—even a "digital" processor has concerns about power supply, heat dissipation, speed, and threshold levels. Digital signal processing is the processing of analog signals by applying *programs*, *logic*, *and symbols* to analog variables in a physical system (such as a radio, camera, or CAT scanner) comprising such analog devices as amplifiers, converters, and DSPs.

So, if the digital world grows, the future must also look bright for analog. But don't take our word for it. As a precursor to the *Dialogue's* fortieth year of celebration, we asked our sage and analog champion, Dr. Barrie Gilbert, ADI Fellow, to look into his crystal ball and give us a vision of the future. In the pages that follow, you will experience a futuristic story he has woven, imagining the pervasiveness and ever-bright possibilities of analog technologies and designs—and their human designers.

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Analog Dialogue

www.analog.com/analogdialogue **dialogue.editor@analog.com**

Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 39 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. In addition to all its current information, the *Analog Dialogue* site has archives with all recent editions, starting from Volume 29, Number 2 (1995), plus three special anniversary issues, containing useful articles extracted from earlier editions, going all the way back to Volume 1, Number 1.

If you wish to subscribe to—or receive copies of—the print edition, please go to **www.analog.com/analogdialogue** and click on **<subscribe>**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com].**

IN THIS ISSUE

No signal chain would be complete without sensors or actuators, and the generic signal chains shown on our four 40th anniversary commemorative covers are no different. The first quarterly issue featured digital signal processors; the second featured A/D and D/A converters; and the third featured amplifiers and linear circuits. This, the fourth and final issue, features the input- and output circuitry.

Few circuits simply crunch numbers—instead they process real-world signals, such as voice, music, or video; or data, such as temperature, pressure, or acceleration. Furthermore, circuits must also communicate with other circuits that may operate in remote locations or hazardous environments. Thus, this issue discusses system considerations encountered in industrial measurement and control, laboratory instrumentation, communications, computers, and other signal-processing applications.

The first article in this issue shows how digital isolators can enable safe transmission of serial data between systems that may be separated by long distances. *Galvanic isolation* is often required to break ground loops, protect the system from high-voltage transients, reduce signal distortion, and enhance physical safety. The digital isolation technology described here uses chip-scale transformers made from CMOS metal layers, plus a gold layer that is placed on top of the passivation. A high breakdown polyimide layer underneath the gold layer insulates the top transformer coil from the bottom. High-speed CMOS circuits connected to the top and bottom coils provide the interface between each transformer and its external signals.

The second article shows how a dual-axis accelerometer can sense an impending crash and protect a personal media player from being destroyed. It describes a novel technique that calculates *differential acceleration* and—if excessive—parks the read/write head of a hard disk drive, thus protecting the head and the platter from damage. The acceleration is sensed by a polysilicon, surface-micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide resistance against acceleration forces. Deflection of the structure is measured using a differential capacitor formed by fixed independent plates in relation to plates attached to the moving mass. The complete single-chip accelerometer includes the sensor and all of the signal-conditioning circuitry required to measure acceleration.

The third article shows how implementing a precision weigh scale may not be as easy as it first seems. Typical weigh-scale resolution is only 1:3,000 to 1:10,000, so a 12-bit to 14-bit ADC would seemingly be adequate. A closer examination, however, shows that a 20-bit ADC is really required. Designers must consider weigh-scale system specifications including noise, dynamic range, offset drift, gain drift, and filtering. The most common weigh-scale implementation uses a bridge-type load-cell sensor, with voltage output directly proportional to the weight placed on it. A typical load-cell is a 4-resistor bridge circuit with at least two variable arms, where the resistance changes with the weight applied, creating a differential voltage at a common-mode level of one-half the supply voltage.

COMING IN 2006

By the end of 2006 we plan to have every issue of *Analog Dialogue* available in our online archives, including all of the rare and long-out-of-print volumes from 1967 on. Also, be on the lookout for a searchable index and perhaps some contests and promotions for you, our loyal readers, to help us celebrate 40 years of *Analog Dialogue*. We welcome your suggestions.

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THE FOUR DEES OF ANALOG, *circa* 2025

By Barrie Gilbert [barrie.gilbert@analog.com]

The young woman standing at the BlueBoard, wearing the least-casual consumables she could find on the cybermall for this important occasion, is Niku Yeng. Aware that every aspect of her interview is being net-vetted—via this fusion of the old whiteboard, HDTV plasma display, two-way mirror, noncontact stress monitor and data link—she is looking a little concerned; but not because of this familiar tool. At the outset, she felt very confident. Her curriculum at Nova Terra University had covered all the major topics of the day. But after an hour of grilling, she felt her hopes of employment at Analog Devices fading, as question after probing question had been so unexpectedly related to fundamental issues.

She'd been asked: "Why are resistors noisy?"; "State the noise-spectral-density of a 50-Ω resistor."; "Show me how the forward voltage of a PN junction varies with temperature."; "What are the essential differences between bipolar transistors—such as today's 25 THz HBTs—and, say, a 10-nm MOS transistor?"; "What causes shot noise?"; "Where do you think the designer of this amplifier got the idea for its topology?" Rather than testing her knowledge of advanced signal processing, modern tools for the rapid realization of microsyms, or even the standard circuit cells in the realm of continuous-value analog (CVA) techniques, the questions seemed aimed at assessing her ability to *invent* circuit solutions—on the spot!—from *fundamental* properties of circuit elements.

This way of thinking about analog design differed greatly from what she'd learned at Nova Terra. Advised of today's extreme emphasis on quick-turn delivery and totally reproducible performance, Niku's emphasis in her Ph.D. thesis was concerned with design and routing tools for F-cell re-use, by developers of microsyms called *Fusers*. (An *F-cell* is a simple functional unit of less than, say, a thousand elements.) Nowadays, the word "transistor" is rarely heard among the Fusers, since the mazes of devices in today's products are merged to the degree that individual elements are indistinguishable. Few Fusers know—or *need* to know—anything about the physical properties of an isolated element. But she was aware that this cannot be said of the *originators*—those who design basic cells from ground zero. It seemed that Analog Devices was currently interested in hiring people of that sort.

Fortunately, her electives had covered the concepts of binary-value analog (BVA—or "binanalog") circuits quite well. She was clear about how the broad class of sigmadel cells work, and familiar with what used to be called "Class-D" amplifiers, using fully switching output devices and duty-cycle modulation—the basis of the sigmadel paradigm—to efficiently deliver generous amounts of audio power. Nowadays, using highly elaborated forms, almost indistinguishable from digital VLSI, binanalog products are ubiquitous. Since about 2010, Class-D amplifiers have been regarded, even by audiophiles, as the most accurate load-driving elements. Sigmadel products using similar output stages now power antennas well into the gigahertz range, thanks to the extremely low inertia of modern transistors and the use of low-loss resonators to convert all the power to the fundamental carrier frequency.

The LEIF (Local E-net Interview Facilitator) turned to probing her perception of how invention and innovation occur in modern companies. Like her fellow students, Niku used the CyberLearn™ system to access an abundance of information. But she's learning from Dr. Leif (coincidentally eponymous) that accumulating information cannot be equated with acquiring knowledge, which is far more profound. Knowledge is about knowing the value of information, skimmed from numerous sources; then filtered, distilled, adapted, extended, assimilated and finally sublimated into a whole, with a set of contextual hooks, in each individual mind, each holding a peculiar world view—a highly differentiated and unique model of reality. "*Knowledge is information activated by thought*," he had told her.

Job interviews aren't usually intended to be mentoring experiences; but Niku was already seeing the prospect of a career in analog design in a new and invigorating light. The old mantra "Analog means antiquated" had emerged from subliminal messages in wave after wave of ads, proclaiming the benefits of "going digital," which conveniently neglected to mention the continued importance of challenges in the real world of analog processors.

"Analog design," said Dr. Leif, "requires one to think in the many dimensions that characterize physical elements and signals. It calls for meticulous attention to minuscule details, always bound by the Fundaments." She'd learned that meant all of the physics of materials and the ground rules governing what can and (probably) cannot be realized in practice. "Analog design can be summed up by the Four Dees, which I briefly mentioned earlier."

Although she'd forgotten what "Four Dees" referred to, the insights gained during the past hour were now illuminating Niku's vision of an exciting future in analog, as an originator. As the interview drew to a close, her eyes twinkling with genuine enthusiasm, she said: "Dr. Leif, thank you for being so generous with your time. I've learned a great deal, and it's apparent you have a deep knowledge of what you call 'The Fundaments.' I'm sure you also have many recollections of the analog world at the beginning of the century. If you'd allow me to buy you coffee at Galaxybux, I'd love to continue this conversation just a little longer."

Leif's smile broadened. Her sincerity and evident zeal fueled his impression that here was more than a talented young lady. She had shown by her answers to many tough questions that she was one of those rarities—a keen problem analyzer and an independent thinker—who compels a manager to give forethought to which of the incentives available to him in acquiring exceptionally talented people he should pick.

"I'd be delighted! I promise not to order anything over $25 a cup!" As they strolled across the campus, he chatted about the microsym business. "That name was suggested by one of the old-timers at ADI decades ago, to capture the notion that the 'ICs' of his time were becoming little cities—microcosms of bustling electronic activity," Leif said. "Today's microsyms have a lot in common with the old silicon ICs, but they no longer depend on the exclusive use of monolithic solutions—which we once thought to be the only way to keep the cost down; that, and the belief that it was imperative to use so-called 'deep submicron CMOS,' which used to mean channel lengths of the order of 100 nm.

"Increasingly, these processes became so severely optimized for binary applications that we needed to re-examine the wisdom of relying on them for high-performance analog signal processing. We realized the flaw in this popular dictate, and went a different way. As you know, our products have for many years combined the unique advantages of a variety of technologies spread out over several smaller chips, each optimally suited to serve the local processing objectives, pre-tested and assembled on tiny substrates entirely automatically using microbots, as you saw earlier today, endowed with a dexterity, speed, and autonomy unimaginable in 2000. Here we are," he said, on reaching the coffee shop.

As they entered, the autowelcomer interrogated the 72-GHz transponder in Leif's pocket. After checking his biometrics, it selected its U.S.-English female voice.

"Hello, Dr. Leif. I heard your team just released another microsym. Congratulations! By the way, have you tried SplendoMix.....?"

Generated by fully analog neural networks, integrated with a local database of customer profiles, these greetings varied intelligently; but the adpops got tiresome after a while. Ordering a Galaxy Express for Leif and a Hitchhiker for herself, charging them via her own transponder, Niku said, "I've read that the price of a coffee has increased 10% per year over the past 20 years, but the price of microsyms continues to decline. Why is that?" Leif smiled with secret pride.

"An astonishing aspect of our industry is that the products keep getting cheaper, in relative terms; and that fact continues to be the key driving force behind today's endless electronic innovations and all the high-tech products they enable. Some of the reasons for this are to be found in the way today's flat-world economy works. But let's just stick to technical matters for now."

"Alright," said Niku, "You briefly mentioned the 'Four Dees of Analog.' I'd like to hear more."

Savoring his espresso, Leif explained, "The Dees are the distinctive differences between the nature of analog and digital design, the products, the components they utilize, and the signals themselves."

"The 'Dees' are the Four Differences, then?" she responded.

"Well, you could say that, but that's not what I have in mind." He took a PDA from an inside pocket. "Let me show you a few slides from a lecture I have on the NovaWeb ... here ... The Dees are mnemonics for capturing these crucial distinctions in four words starting with that letter. They're equally important, but let's start with one that touches on that issue of economy.

"Analog microsyms are DURABLE. Very successful products can have a lifetime of over thirty years."

"I'm surprised!" she replied. "From what I learned at college, a lifetime of a few years is generally the case for VLSI, before they're outdated by a new technology. Why doesn't that impact analog in the same way?"

"A good question, one not easy to answer. It's partly because analog functions still tend to be generic in spite of many examples of very complex and specialized analog products designed for a specific service. But while the latter may include scores of amplifiers, there are still uses for single units. A good all-rounder, well-designed in an older technology, eventually becomes so cheap—a penny or two—that it continues to find applications in many places. Unlike, say, a binary AND gate, which is far too primitive a function to make as a standalone part, an amplifier actually serves each application differently, and there's no need for the fastest technology in many of them. It's also a reflection of the three other Dees."

"This is fascinating! I've never thought about analog design at such a basic level as you've presented. I thought it was all re-use, now," said Niku, with evident delight. "What's the second Dee?"

Touching the screen of his PDA, Leif retrieved another slide. Underneath a row of notes on a music staff, it said DIVERSE.

"What does that mean?"

It was Leif's turn to show signs of delight. Speaking with boyish glee, "Analog design is all about writing new tunes. You see this row of just 16 notes, equal in duration? Suppose each has one of 20 allowable pitches. How many tunes can you write?"

"Hundreds, I imagine!"

"How about 655 billion-billion? The notes are your components; but today's tunes—that is, the cell topologies—use many more than 16 components, and each can have far more than 20 'pitches'—the parametric variations. Not all these combinations are useful, of course, just like the tunes; but in practice there are still endless opportunities for invention."

"That's a wonderful metaphor, Dr. Leif." Suddenly, the coffee-shop lights flickered and died. "Well!" she laughed, "*that's* a digital problem!"

"You're probably right—I've heard that the control systems for these latest white emitters have some software bugs. But you can still see my PDA, right?" The screen showed the word DIMENSIONAL, above which was a list of several signal parameters—voltage, current, frequency and so on; and below, component parameters, including resistance, capacitance, and inductance. All were defined in terms of just four dimensions in the modified MKS system: mass, time, length, and charge. "Now, this is the most profound difference." Then teasingly, Leif said "Tell me: What is the dimension of a logical variable?" Niku was not to be caught off-guard.

"Well, it doesn't have any dimension!"

"Right! So given that latitude, why are we still using very similar elements for digital processors as we use for analog?"

"Well, they are very cheap, very tiny, and very fast."

"Right again! But why haven't all those other nanodevices stepped in, to replace silicon?"

"Economics?"

"Exactly! Even though digital processors are only incidentally electronic, silicon is a very serviceable medium. On the other hand, analog circuits are fundamentally dimensional: their performance depends on the quality, actual physical size, and absolute value of the components, so the designer must be constantly aware of the consequences of misjudging such factors."

"Well, component matching is important too."

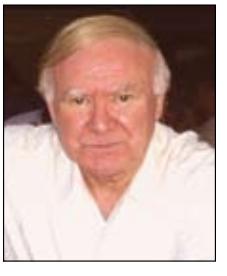
"Yes, that's true; but matching like against like is a dimensionless proposition. You see, there are two kinds of sensitivity in an analog circuit: aspects of performance that are *dependent on* absolute parameter values, and those that are *tolerant of variations* in absolute values." At that moment, the lights came back on, and Niku asked whether Dr. Leif would like another Galaxy Express.

"Thank you, but I have to get back to the lab."

Disappointed, she said, "But aren't you going to tell me what the Fourth Dee is?"

"No, not right now. Let's continue this conversation at our website: <www.analog.com/library/analogdialogue/leif1.html>. You must excuse me. By the way," he said, as he started from the table, "I would be honored if you should wish to join my team."

And Niku felt sure the white emitters flickered.



Barrie Gilbert, the first-appointed ADI Fellow, has "spent a lifetime in pursuit of analog excellence." Barrie was born in Bournemouth, England, in 1937. Before joining ADI, he worked with first-generation transistors at SRDE in 1954. At Mullard, Ltd. in the late '50s, he pioneered transistorized sampling oscilloscopes, and in 1964 became a leading 'scope designer at Tektronix. He spent two years as a group leader at Plessey Research Labs before joining Analog Devices in 1972, where he is now director of the Northwest Labs in Beaverton, Oregon. Barrie is a Life Fellow of the IEEE and has received numerous service awards. He has about 70 issued patents, has authored some 50 papers, is a reviewer for several professional journals, and a co-author or co-editor of five books. In 1997, he was awarded an honorary doctorate of engineering from Oregon State University.

*i*Coupler® Digital Isolators Protect RS-232, RS-485, and CAN Buses in Industrial, Instrumentation, and Computer Applications

By Scott Wayne [scott.wayne@analog.com]

INTRODUCTION

In applications such as industrial process control, power supply regulation, and point-to-point communications between computers, serial communication buses transmit data over various types of physical networks, such as RS-232, RS-485, and the *Controller Area Network* (CAN). Each of the interconnected systems usually has its own power supply, and the systems are often separated by long distances, so galvanic isolation is typically required to break up ground loops, protect the system from high-voltage transients, and reduce signal distortion, as well as for physical safety.

Isolation

Transformers, coupling capacitors, optocouplers—and now, *i*Couplers—are typical means of providing galvanic isolation, which blocks current from flowing between two points, while allowing data to pass unimpeded (Figure 1). Isolation is used to protect against high voltages or currents caused by line surges or ground loops, which can occur in any system that has multiple ground paths. System grounds that are separated by long cables will not be at the same potential, so ground current will flow between the two systems. Without isolation, this current could introduce noise, degrade measurements, or even destroy system components.

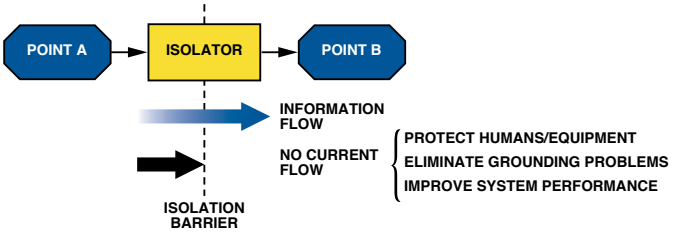


Figure 1. Galvanic isolation allows information flow but prevents current flow.

Currents that are inductively coupled into the long cables found in industrial environments by motors switching *on* and *off*, electrostatic discharge (ESD), or nearby lightning strikes can cause rapid changes in ground potential, often as large as hundreds, or thousands, of volts. When this occurs, the logic-level switching signal expected by the remote system would be superimposed on a high voltage with respect to its local ground. Without isolation, this voltage could corrupt the signal or damage the system. Referring all devices connected to the bus to a single ground will protect the system against this destructive energy, and isolating the devices will prevent ground loops and electrical surges.

To completely isolate the system, *all* signal lines and power supplies must be isolated. An isolated dc-to-dc converter can provide power supply isolation, while the *i*Coupler digital isolator provides the signal isolation.

*i*Coupler Technology

*i*Coupler isolators are magnetic couplers based on chip-scale transformers (Figure 2), as compared with the LEDs and photodiodes used in optocouplers. The planar transformers use CMOS metal layers, plus a gold layer that is placed on top of the passivation. A high breakdown polyimide layer underneath the gold layer insulates the top transformer coil from the bottom. High-speed CMOS circuits connected to the top and bottom coils provide the interface between each transformer and its external signals. Wafer-scale processing provides a low-cost method for integrating multiple isolation channels, as well as other semiconductor functions, in a single package. *i*Coupler technology eliminates the uncertain current transfer ratios, nonlinear transfer functions, and drift (with time and temperature) associated with optocouplers; reduces power consumption by as much as 90%; and eliminates the need for external drivers or discrete devices.

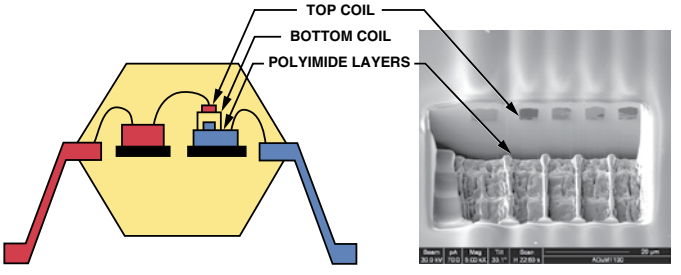


Figure 2. *i*Coupler cross section.

Circuitry on the primary side of the transformer encodes the input logic transitions into 1-ns pulses, which are then coupled through the transformer; circuitry on the secondary side detects them and recreates the input signal, as shown in Figure 3. A *refresh* circuit on the input side ensures that the output state matches the *input* state even if no input transitions are present. This is important in *power-up* situations and for input waveforms with low data rates or constant dc inputs.

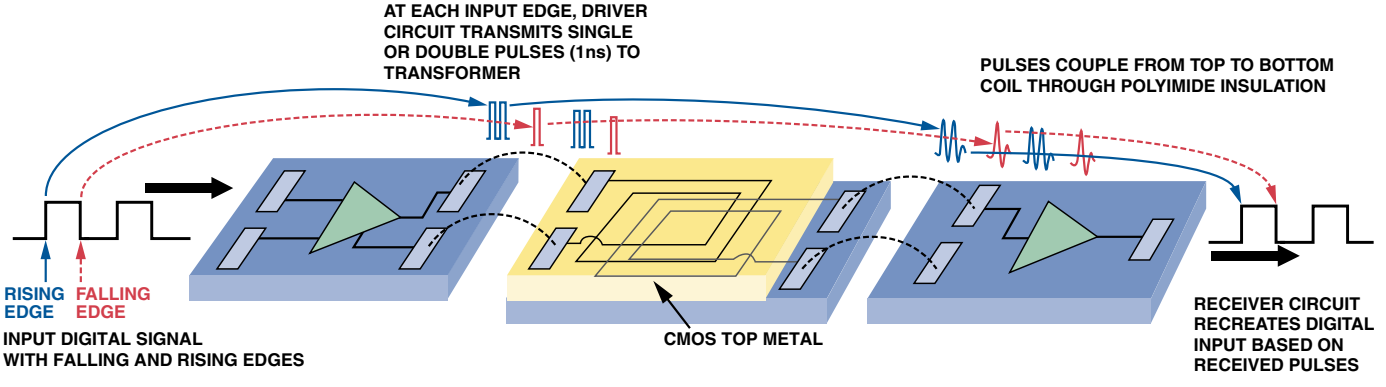


Figure 3. The digital input is recreated at the output of the *i*Coupler.

Because the purpose of *i*Coupler products is to isolate an input from an output, the circuitry on one side of the transformers must be contained on a separate chip from the circuitry on the second side of the transformers. The transformers themselves can be placed on either chip—or on a third chip, as in the ADuM140x[1] shown in Figure 4. The entire chipset is assembled within a standard plastic package similar to that used for a wide variety of semiconductor devices.

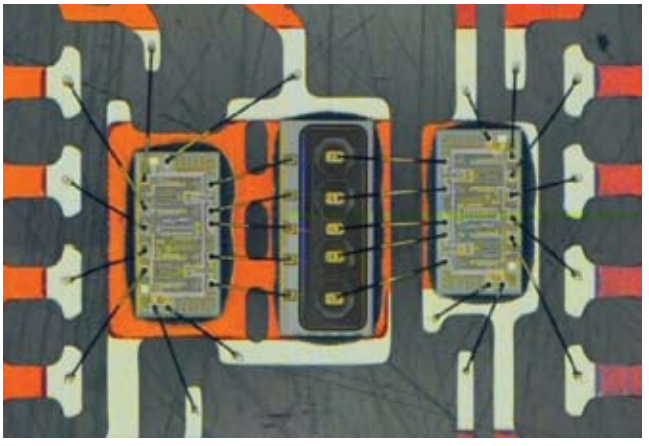


Figure 4. ADuM140x 4-channel isolator construction.

A novel feature of *i*Coupler devices is their ability to combine both *transmit* and *receive* channels in the same package. The *i*Coupler transformers are inherently bidirectional, so signals can pass in either direction as long as the appropriate circuitry is present on each side of the transformers. In this manner, multichannel isolators are offered with a variety of transmit/receive channel configurations.[2]

Serial Communication Buses

RS-232 (EIA232) and RS-485 (EIA/TIA485) specifications define the physical layer only, allowing the signal protocol to be defined by the user, or by other standards that specify their use in the physical layer. On the other hand, the CAN bus defines both the physical layer and the data link layer.

RS-232: The RS-232 bus standard, one of the most popular serial communication buses, was originally specified in 1962 for communication between computers and modems. Still widely used as an intersystem communication link, its simplicity, flexibility, and long history of successful use account for its continued popularity. Designed for point-to-point communications, it provides full-duplex communication using two dedicated, unbalanced single-ended lines with ground-referred signals.

Data rates are limited to 20 kbps, or 64 kbps in a low-voltage variation. The maximum practical cable length is limited to about 16 meters by the 2500-pF maximum load capacitance and the 3-kΩ to 7-kΩ load impedance. RS-232 specifies *driver* output levels of –5 V to –15 V for Logic 1 and +5 V to +15 V for Logic 0—and receiver input levels of –3 V to –15 V for Logic 1 and +3 V to +15 V for Logic 0. Voltages between –3 V and +3 V are undefined. The wide voltage swing and undefined region ensures a high level of noise immunity and allows valid signal levels to be received over lengthy cables.

The RS-232 specification defines the pinout for a 25-pin D connector with 20 signal lines, but the 9-pin connector with eight signal lines, shown in Figure 5, is more common. One line in each direction is used for data transmission; the remaining lines are designated for the communications protocol. At its simplest, RS-232 can be implemented with just three lines: *Tx* (transmit data), *Rx* (receive data), and GND (ground). A protective ground, used for equipment safety, is defined in the 25-pin connector. This line, typically connected to the power ground or chassis ground, should not be connected to the signal ground or from system to system.

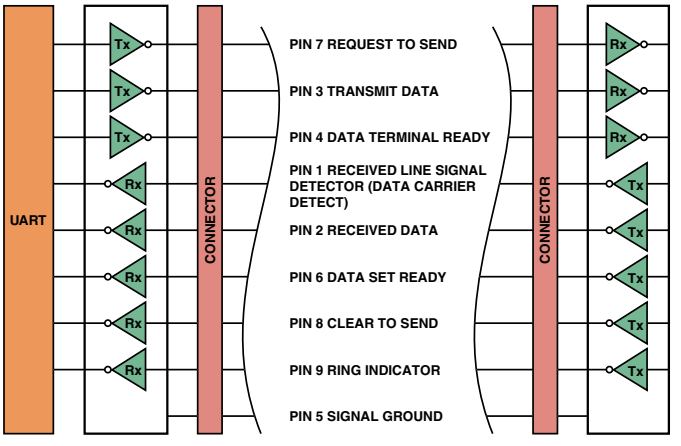


Figure 5. 8-signal RS-232 network configuration.

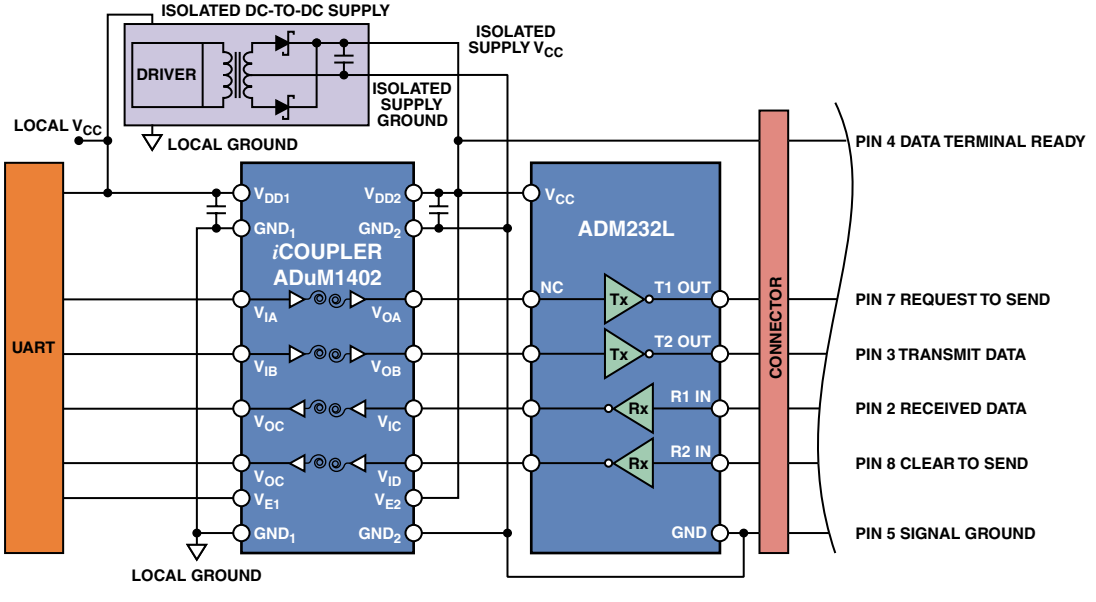


Figure 6. 5-signal isolated RS-232 circuit (DTE side illustrated).

The RS-232 standard divides equipment into two categories: DCE (data communications equipment) and DTE (data terminal equipment). These designations are a legacy of their computer and modem heritage; the terms now simply define which lines are connected as inputs and which are connected as outputs.

RS-232 is typically used to connect multiple systems, so isolation between each system and the bus is critical. Digital isolators do not support the RS-232 standard, so they cannot be used between the transceiver and the cable; instead they are used between the transceiver and the local system. The *system* side of the transceiver typically connects to a universal asynchronous receiver/transmitter (UART) or a processor, using 0 V to 3 V or 0 V to 5 V logic levels. Because the input and output circuits of the *i*Coupler isolator are electrically isolated from each other, one can be placed between the UART and transceiver as a simple way of isolating the system from the cable. To complete the isolation, an isolated dc-to-dc converter is used to supply power to the isolator and transceiver. The combination of the ADuM1402[3] *i*Coupler digital isolator, ADM232L[4] RS-232 transceiver, and isolated power supply, shown in Figure 6, eliminates ground loops and provides effective protection against surge damage.

RS-485: The RS-485 standard is specified to drive up to 32 pairs of drivers and receivers. Its versatility and ability to drive 4000-meter cables make it popular for a wide range of applications, especially for interconnecting systems over very long distances. The *Small Computer Systems Interface* (SCSI) and PROFIBUS protocols both use RS-485 for communications.

Usable cable lengths are dependent upon data speed requirements, with speed/length combinations ranging from 200 kbps at 1200 meters to 12 Mbps at 100 meters. Using balanced differential signaling, RS-485 drivers send data across two output lines. The receiver determines the logic state by comparing the two signals; a difference greater than 200 mV provides a valid logic level. Differential amplifiers in the drivers and receivers steer current between the signal lines. This provides a high level of noise immunity in comparison with single-ended schemes such as RS-232.

An *enable* function allows the drivers to be put into a high-impedance state; so multiple drivers can share a single bus without contention. The software protocol defines the bus arbitration procedure, keeping all but one driver inactive at all times and allowing line-sharing by up to 32 drivers. A half-duplex, 2-wire bidirectional configuration is shown in Figure 7. Each node contains a driver and receiver, with all drivers and receivers sharing the same 2-wire twisted-pair cable. While this simplifies installation and reduces cost, it limits the maximum throughput rate. A 4-wire full-duplex configuration—using one node as a master and the remaining nodes as slaves—is more complex but provides higher data rates.

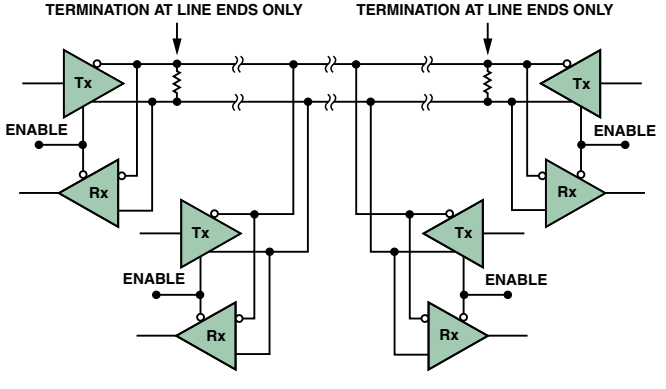


Figure 7. 2-wire, multidrop, half-duplex RS-485 network.

Because RS-485 is typically used to connect multiple systems, isolation between each system and the bus is critical. As with RS-232, digital isolators do not support the RS-485 standard, so they cannot be used between the transceiver and the cable; instead they are used between the transceiver and the local system. The *system* side of the transceiver typically connects to the local bus or a processor. Since the input and output circuits of the *i*Coupler isolator are electrically isolated from each other, interposing one between the processor and transceiver is a simple way of isolating the system from the cable. To complete the isolation, an isolated dc-to-dc converter is used to supply power to the isolator and transceiver. The combination of ADuM1301[5] *i*Coupler digital isolator and isolated power supply shown in Figure 8 eliminates ground loops and provides effective protection against surge damage.

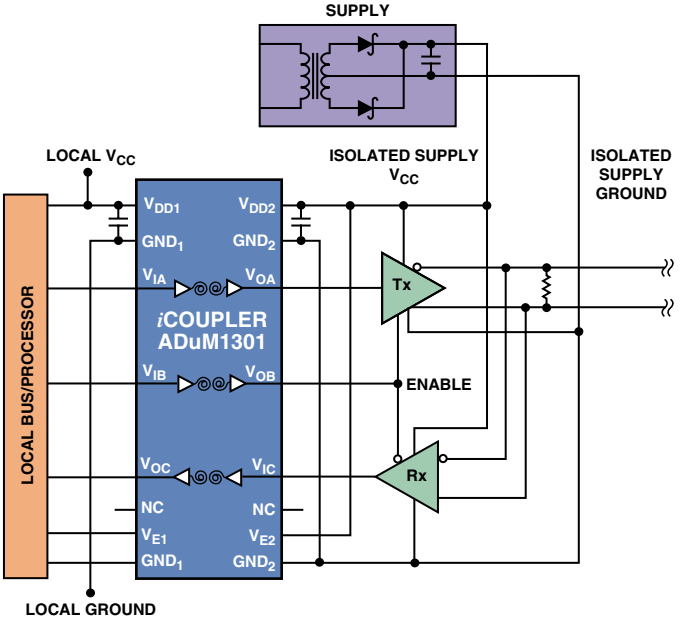


Figure 8. Isolated RS-485 circuit.

Figure 9 shows the ADM2486[6] single-chip isolated RS-485 transceiver.

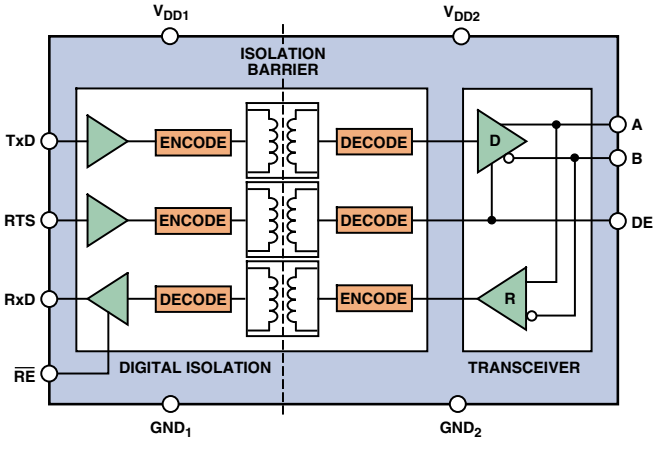


Figure 9. ADM2486 isolated RS-485 transceiver.

CAN Bus: The CAN bus standard, originally developed for automotive applications, specifies a 2-wire serial communications protocol that allows data rates up to 1 Mbps, with up to 30 nodes and a 40-meter maximum cable length. It transmits asynchronous data in frames that consist of *start* and *stop* bits, an arbitration field, a control field, a cyclic redundancy check (CRC) field, and

an *acknowledge* field. Every node can listen and transmit at the same time, so one of the most important features of the protocol is its nondestructive bit arbitration, which ensures that no data is lost. Each node transmits a dominant *start of message* (SOM) bit at the beginning of each message. Other nodes will see this activity and will not attempt to start a transmission until the message is complete. Next, the 11-bit or 29-bit arbitration field is transmitted. Also known as the identifier, this field prioritizes the messages sent on the bus. The highest priority node always takes control of the bus, leaving lower-priority nodes to wait. This nondestructive arbitration ensures that the highest priority message always gets through.

The CAN bus, shown in Figure 10, uses a balanced, 2-wire differential interface and typically operates at 3 V or 5 V. *Non-return-to-zero* (NRZ) encoding is used, ensuring compact messages with a minimum number of transitions and high noise immunity. CAN bus transceivers use a pair of open-drain devices to create a differential signal of CANH (V_{CC} – 0.9 V) to CANL (1.5 V). When driven, the transmitter produces the dominant signal, which represents a logic *low*. When no transmitter is driven, pull-up resistors set the bus to $V_{CC}/2$, producing the recessive signal, which represents a logic *high*. A *standby* control puts the transceiver into a low-power mode. A low-power receiver remains active during standby mode, monitoring the bus for state changes—and signaling the controller to activate the local node when activity is detected.

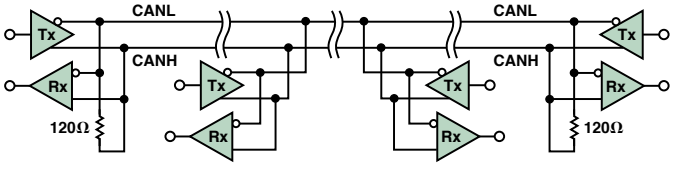


Figure 10. CAN bus network.

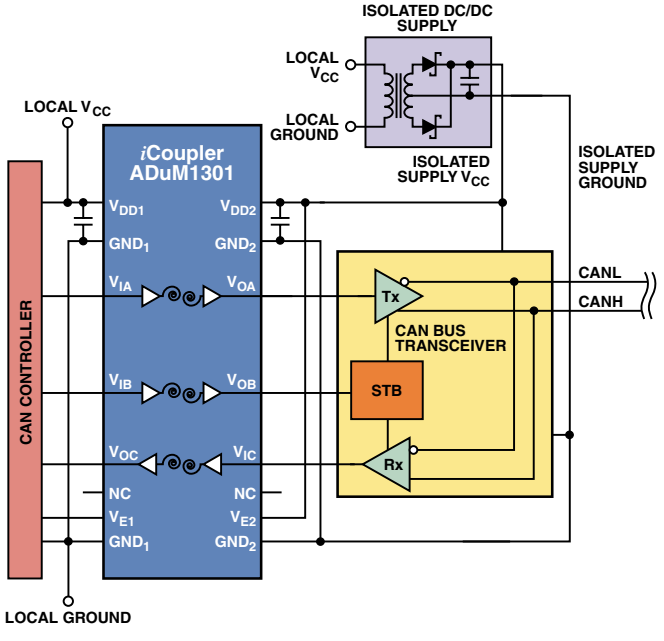


Figure 11. Isolated CAN bus network.

As with RS-232 and RS-485, digital isolators do not support the CAN bus standard, so they cannot be used between the transceiver and the cable; instead they are used between the transceiver and the local CAN controller using standard 3-V or 5-V logic levels. Because the input and output circuits of the *i*Coupler isolator are electrically isolated from each other, a simple way of isolating the system from the cable is to interpose one between the processor and transceiver. To complete the isolation, an isolated dc-to-dc converter is used to supply power to the isolator and transceiver. The combination of *i*Coupler digital isolators and an isolated power supply, shown in Figure 11, eliminates ground loops and provides effective protection against surge damage.

More About *i*Couplers

Digital isolators based on *i*Coupler technology can be compared favorably with optocouplers in terms of integration, performance, power consumption, ease of use, and reliability. *i*Coupler devices are self-contained, requiring no extra components except for the usual bypass capacitors; they are generally faster, with higher data rates (to 100 Mbps) and shorter propagation delays (18 ns); their power consumption (from 5 mW @ 1 Mbps to 22 mW @ 25 Mbps) is from 1/70 to 1/5 that of comparable optocouplers, with negligible heating of adjacent components; they can be used in the same way as standard digital CMOS; they can work at higher temperatures—with propagation delay essentially insensitive to temperature; and they have increased lifetimes, without LED wearout. They have similar safety approvals to high-quality optocouplers. Currently available *i*Coupler devices have insulation rated at 2.5 kV rms (400 V rms steady state), with prospects of better than 50% future improvement.

Full Disclosure

Since *Analog Dialogue* is not a cookbook, these examples basically illustrate how *i*Coupler technology can be used in network communications; they are not detailed schematics of tested applications. Please consult product data sheets and any available application notes (see below) for more information. As always, *use extreme caution when working with high-voltage circuits.*

FOR FURTHER READING

AN-727: *i*Coupler Isolation in RS-485 Applications.

AN-740: *i*Coupler Isolation in RS-232 Applications.

AN-770: *i*Coupler Isolation in CAN Bus Applications.

Frequently Asked Questions About Isolation, *i*Coupler Technology, and the ADuM1100 Digital Isolator.

*i*Coupler Digital Isolation Products.

*i*Coupler Isolation Technology.

*i*Coupler Product Family.

Wayne, Scott. "Finding the Needle in a Haystack." *Analog Dialogue* 34-01. January-February 2000.

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[2] http://www.analog.com/Analog_Root/static/pdf/dataConverters/SelectionGuides/digitalIsolators.pdf

[3] ADI website: www.analog.com (Search) ADuM1402 (GO)

[4] ADI website: www.analog.com (Search) ADM232L (GO)

[5] ADI website: www.analog.com (Search) ADuM1301 (GO)

[6] ADI website: www.analog.com (Search) ADM2486 (GO)

This article can be found at http://www.analog.com/library/analogdialogue/archives/39-10/iCoupler.html, with a link to a PDF.

Using Dual-Axis Accelerometers to Protect Hard Disk Drives

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INTRODUCTION

Hard disk drives (HDDs) are becoming more widely used than ever before, due to the explosive growth in the introduction of portable equipment such as laptop computers, portable media players (PMPs), and handsets. As more and more devices incorporate HDDs, the need has become more pressing to protect them from shocks produced by severe impacts when a product that contains one is dropped accidentally. To increase the ability of HDDs to survive such events, their impact resistance must be enhanced.

There are two approaches to establishing the necessary impact resistance, *active* and *passive*.

Passive approaches have been in use for a long time; they simply cushion the device with impact-absorbing materials,[1] usually rubber or gels. Gels, which tend to be better able to absorb an impact, are more widely used than rubber. However, gels cannot protect devices from damage caused by falls of more than one meter; this precludes their use in portable entertainment equipment. Devices such as handsets, MP3 players, and PMPs need to be protected for a drop of more than 1.5 meters (the average height of a human ear above the ground).

Among *active* approaches, there are two alternatives for protecting HDDs. One is to increase cache memory capacity so that the HDD is in a *read* or *write* mode less often. This approach would also reduce power consumption and heating. But it is costly and fails to deal with the impact that can occur should the HDD be in a *read* or *write* mode at the instant the fall begins. The second approach is to employ accelerometers (such as the Analog Devices ADXL320 dual-axis accelerometer,* which measures axial acceleration) to detect a drop and then generate a signal that causes an HDD head to be recalled to a safe zone. If this can occur before the product hits the floor or other stationary surface, a collision between head and platter will be prevented. This approach was first used commercially in a notebook PC released by IBM in October 2003.

Modeling Free Fall

The simplest model for free fall of an object is depicted in Figure 1, where the Z axis of the falling object is assumed to be perpendicular to the surface of the earth.

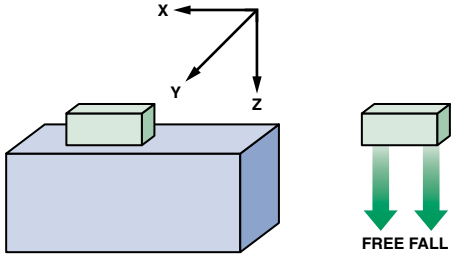

Figure 1. Special case of the free-fall model—acceleration confined to a single axis.

In Figure 1(a) the object is assumed to be stationary, so that the accelerations along the X and Y axes are both zero, hence the force along the Z axis, governed by Newton's second law, will have the value of 1 *g* (32.174 feet-per-second per second at sea level), corresponding to the stationary acceleration force due to gravity.

In Figure 1(b) the object is allowed to fall. The accelerations along the X and Y axes remain the same, zero *g*, but now the accelerometer that measures acceleration along the Z axis, being accelerated at the same rate as the object to which it is fastened, will record a value of zero *g*.

A more general case for a falling object is shown in Figure 2. Here the edges of the cube form arbitrary angles with regard to the orthogonal coordinate system.

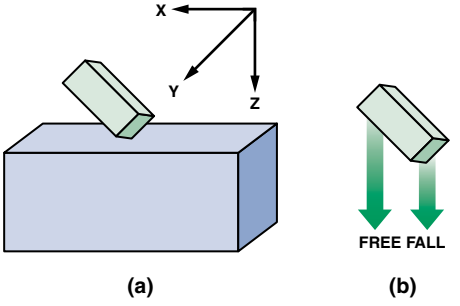

Figure 2. Generalized free-fall model—acceleration components along all three axes.

In Figure 2(a), the object is depicted in a generalized arbitrary orientation; its edges form angles α, with respect to the X axis; β, with respect to the Y axis; and γ, with respect to the Z axis. At zero-*g* acceleration, the voltage output of each axis sensor is $V_{CC}/2$. Accordingly, the outputs for the three axes will be:

$$X\ output = V_{CC}/2 \pm \left[\left(sensitivity\right)\left(1g\right)\left(\sin\alpha\right)\right] \quad (1a)$$

$$Y\ output = V_{CC}/2 \pm \left[\left(sensitivity\right)\left(1g\right)\left(\sin\beta\right)\right] \quad (1b)$$

$$Z\ output = V_{CC}/2 \pm \left[\left(sensitivity\right)\left(1g\right)\left(\cos\gamma\right)\right] \quad (1c)$$

"Sensitivity" refers to the output of the sensor per *g*. For the ADXL320, when powered by +3 V, the sensitivity will be 174 mV/*g*. If the direction of the detected linear acceleration corresponds with the positive direction of a coordinate axis—X, Y, or Z—its sign will be positive and its output will add to $V_{CC}/2$; otherwise it will be negative and will subtract from $V_{CC}/2$.

When the object is dropped suddenly, the accelerations along all three axes become zero because, regardless of the orientation of the object to the coordinate system, no acceleration will be detected along any axis since, as explained above, the accelerometer is accelerating towards the earth at the same rate as the falling body.

For portable equipment, we must also consider any angular acceleration that may be imparted to the object, as shown in Figure 3.

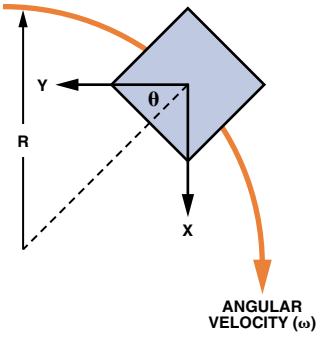

Figure 3. Angular acceleration of a falling object.

*See sidebar on page 12.

In order to simplify the calculation of the angular acceleration, the analysis will be confined to the plane determined by the X and Y axes, thereby simplifying the analysis.

If the angular velocity is ω and the radius of rotation is *R*, then the angular acceleration (A_C) is:

$$A_C = \omega^2 R \tag{2}$$

Therefore, the components of the angular acceleration along the X and Y axes will be:

$$A_{CX} = \omega^2 R \sin\theta \tag{3a}$$

$$A_{CY} = \omega^2 R \cos\theta \tag{3b}$$

So, in reality, the falling body will exhibit both linear acceleration and angular acceleration, a combination of the various cases discussed above.

To compute the time that will elapse when an object falls, starting with a velocity of zero perpendicular to the earth at the instant of the fall, we can use the following equation based upon Newton's second law of motion:

$$t = \sqrt{\frac{2h}{g}} \tag{4}$$

where *h* is the height of the fall and *g* is the gravitational acceleration, 32.174 feet/second/second.

To get a sense of the time available to respond to a fall, we can assume a height of 3 feet. Using equation (4), time = 432 ms.

A Traditional Protection Algorithm

Traditionally, the HDD protection algorithm has been based on free-fall modeling, as explained below, in which the outputs of the sensors contained in the accelerometers can be easily captured by a digital oscilloscope or other data sampling system.

A "test sled" can be assembled using two ADXL320[2] dual-axis accelerometers. The axes of the accelerometers are aligned with the X, Y, and Z axes, as depicted in Figure 4, thereby providing values of acceleration along the X, Y, and Z coordinates. (The Y_1 output is redundant and is not used.) The outputs of the coordinate axes are sampled by a 12-bit ADC contained in an ADuC832[3] precision analog microcontroller, which integrates the sampled data and feeds it to an internal 8052-compatible core processor. The sampled data is then transferred to the computer—via an RS-232 interface—for analysis.

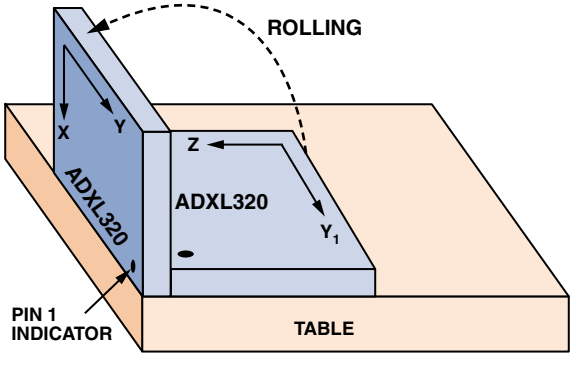

Figure 4. The test sled.

Figure 5 shows the sequence of responses sensed by the two sensors. Values X and Y are supplied by one accelerometer, the values Z and Y_1 are supplied by the other accelerometer. Note also that the plot is divided into four consecutive intervals labeled: "static," "rollover," "free-fall drop," and "impact." The sampling interval, shown along the X axis, is determined by the ADC, which is clocked at 200 Hz for each variable, or one sample of each variable every 5 milliseconds. The Y-axis scale represents the values delivered by the 12-bit ADC in the ADuC832 smart-transducer front end, plotted for all four axes.

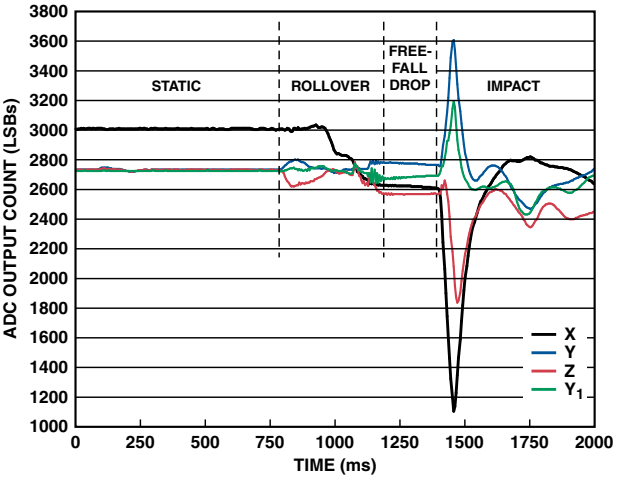

Figure 5. Traditional protection algorithm—sequence of responses sensed by the accelerometers.

The test sled, placed at the edge of the table and caused to roll over, imparting angular acceleration—as depicted in Figure 4—produces the rollover data shown in Figure 5. (The Z-axis value, apparently not-equal-to-zero-*g* output in static mode, is caused by the unbalanced installation of the accelerometer.)

When the sled is pushed off the table, the values are all constant near their respective zero levels during this free-fall-drop interval, in line with the above assertion that during the free fall the outputs of all the accelerometers will be zero-*g* output.

(Note also that the zero-*g* output for the accelerometers along different axes in the same time interval is not quite the same.)

The traditional HDD protection algorithm is based on the data obtained in the arrangement just described. The system monitors the acceleration along the X, Y, and Z axes of the object. If the root-sum-of-squares value calculated from Equation 5 is equal to or less than the threshold value, a signal is sent to the computer associated with the HDD causing the head to park safely before the portable device collides with the floor.

$$\sqrt{X^2 + Y^2 + Z^2} \leq \text{Threshold} \tag{5}$$

The choice of the threshold value is governed by the specific response-time requirement, as well as the sensor's parameters—such as sensitivity, sensitivity change due to temperature, operation voltage, noise density, package alignment error, sensor resonant frequency, and the working temperature range of the equipment. Normally, the threshold value can be determined from experiments, like the one described above. For example, a designer might choose a threshold value of 0.4 *g*.

A New Differential Acceleration Algorithm

Now let's look more closely at the behavior of the acceleration plots in Figure 5. If sufficient information to distinguish a fall were to be obtained during the rollover interval, there would be much more time available for protective action by the computer. In fact, the sensor outputs do vary during that interval, but the output values are not sufficiently pronounced to directly initiate the HDD protection process.

However, if a new function is formed, equal to the sum of the squares of the time derivatives of the X- and Y-axis accelerometer outputs (Equation 6),

$$\left(\frac{dX}{dt}\right)^2+\left(\frac{dY}{dt}\right)^2 \text{ or } \left(\frac{dZ}{dt}\right)^2+\left(\frac{dY_1}{dt}\right)^2 \quad (6)$$

the results obtained will be as depicted in Figure 6. The values plotted in Figure 6 are the results of calculations based on outputs from the 12-bit ADC in the ADuC832 smart transducer front end. The sample numbers are again in 5-ms time increments. The black plot is the instant-by-instant value of $(dX/dt)^2 + (dY/dt)^2$, and the green plot is the instant-by-instant value of $(dZ/dt)^2 + (dY_1/dt)^2$.

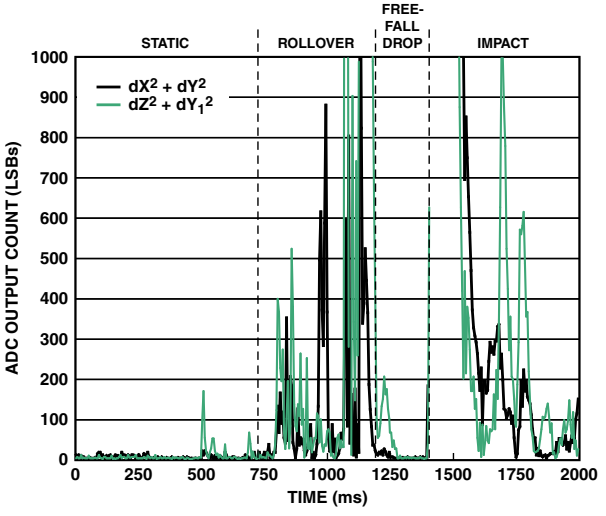

Figure 6. Differential acceleration algorithm-time-derivative plots for $(dX/dt)^2 + (dY/dt)^2$ and $(dZ/dt)^2 + (dY_1/dt)^2$.

As expected, the sums of the squares of the time derivatives are quite large during the rollover time interval, but they become quite small during the free-fall drop. This sequence of events can be employed to provide a reliable indication that a fall has occurred.

It is important to note that our research confirmed that either of the two accelerometers can be chosen, since they provide similar behavior. So the choice of the sensor axes to be monitored can be arbitrary.

We can now establish a new test algorithm, labeled "the *differential acceleration* algorithm" (Equation 7):

$$\left(\frac{dX}{dt}\right)^2+\left(\frac{dY}{dt}\right)^2 < \text{Threshold} \quad (7)$$

The threshold of the time differential of sensor outputs, the key for the dropping detection, is related only to the sensitivity of the sensors. With the ADXL320, for example, the threshold can be selected as 200 counts (on the number scale used by the algorithm).

Implementing the Differential Acceleration Algorithm

The principal components of a system to implement the differential acceleration algorithm are an ADXL320 dual-axis accelerometer, an AD8542[4] dual rail-to-rail amplifier and an ADuC832 smart transducer front end.[2,3,4] A simplified schematic of the system appears in Figure 7.

The signals from the accelerometer are fed via the AD8542, which serves as a buffer between the accelerometer outputs and the ADuC832's inputs, ADC0 and ADC1. A multiplexer switches between the two inputs at a rate of 200 samples per second for each channel, continuously monitoring the arriving acceleration signals.

The 8052 microcontroller core, which is a component of the ADuC832, implements the algorithm diagrammed in Figure 8. Then, whenever the system detects that a fall has occurred, a general I/O feeds an alert signal to the companion computer of the HDD so that the HDD will safely park the hard-disk-drive head before an impact occurs.

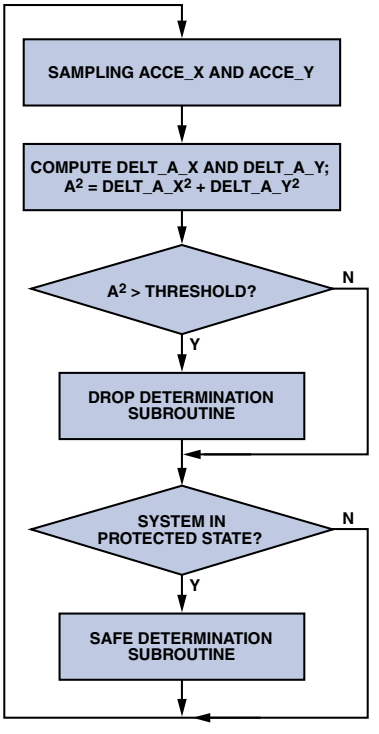

Figure 8. Differential acceleration algorithm—HDD-protection flow chart.

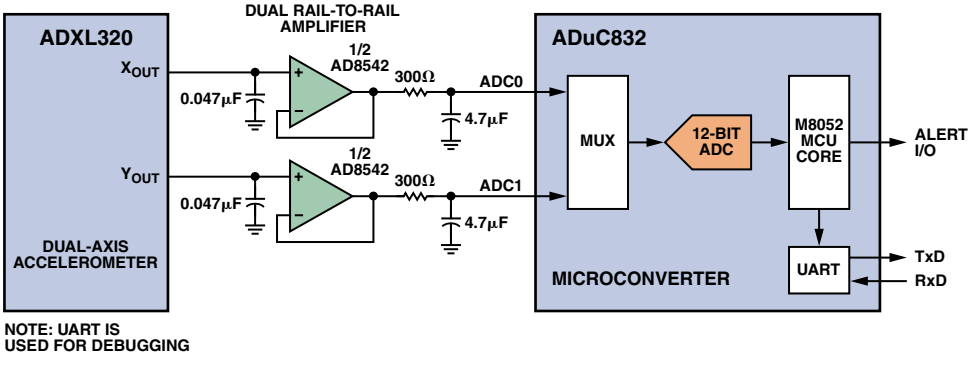

Figure 7. Simplified schematic of HDD-protection hardware system.

CONCLUSION

One might ask whether a tri-axis sensor is essential for HDD protection. The answer is *no*. For, as demonstrated above, the use of an ADXL320 *dual-axis* accelerometer, when employed in a protection system that implements the *differential acceleration algorithm* discussed above,* performs the task quite ably. In addition to lower cost, the dual-axis sensor approach saves space and reduces power dissipation.

Based on the HDD protection system we built, it has been found that the response time between the instant a free fall occurs and the time the alert signal is generated will be 40 milliseconds, with a sampling rate of 200 samples per second per channel and a sensor bandwidth of 100 Hz. The time required to park a hard-disk-drive head should not exceed 150 ms in order to lower the cost of the whole system. Therefore, the total time from a detected free fall to the completion of the parking is no more than 190 ms. This is far less than the 432 ms that it takes for a portable product to fall 3 feet.

The algorithm described in this article is applicable for almost all the cases described above. The only case that it cannot detect is a free-fall event in which the time derivatives of the squares of the sensed X and Y accelerations at the instant that the fall occurs remain negligible during the free-fall drop. But this is quite unlikely, and, in our experience, it has never occurred.

ACKNOWLEDGEMENTS

The authors would like to thank Harvey Weinberg and Christophe Lemaire for their technical expertise. The authors also would like to thank Justin Littlefield and Steve Grossman for assistance in writing this article.

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[3] ADI website: www.analog.com (Search) ADuC832 (GO)

[4] ADI website: www.analog.com (Search) AD8542 (GO)

*Patent applied for.

THE ADXL320 2-AXIS ACCELEROMETER

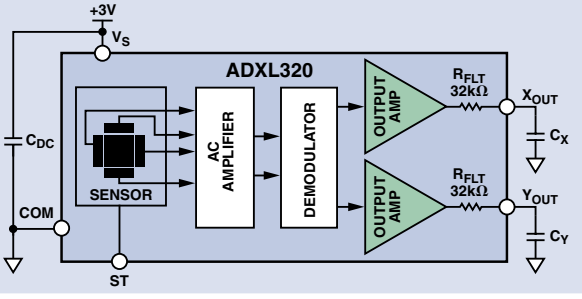
The Analog Devices ADXL320 is a low-cost, low-power, dual-axis acceleration measuring system with signal-conditioned voltage outputs, all on a single monolithic IC. The product measures acceleration with a full-scale range of ±5 *g* (typical). The ADXL320 is housed in a very-thin, 4-mm × 4-mm × 1.45-mm, 16-lead plastic LFCSP.

The accelerometer contains a sensor and signal-conditioning circuitry to implement an open-loop acceleration measurement architecture. The output signals are two analog voltages proportional to the orthogonal accelerations.

The sensor is a polysilicon, surface-micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide resistance against acceleration forces. Deflection of the structure is measured using a differential capacitor formed by fixed independent plates in relation to plates attached to the moving mass.

The fixed plates are driven by square waves which are 180° out of phase. When the device is subjected to an acceleration force, the beams deflect, unbalancing the differential capacitor—which results in an output square wave with amplitude proportional to acceleration. Phase-sensitive demodulation circuitry, contained in the demodulator block in the illustration, is then used to rectify the signal and determine whether the acceleration is positive or negative.

The demodulator's measured accelerations, along the X axis and Y axis of the ADXL320, are amplified by the output amplifiers and brought off-chip through 32-kΩ resistors, as shown in the illustration. External capacitors can be used to provide filtering.



ADXL Low-*g* Accelerometer Selection Table

Part Number	No. of Axes	Range (*g*)	Sensitivity	Sensitivity Accuracy (%)	Output Type	**Max Bandwidth (kHz)	Noise Density (µ*g*/√Hz)	Voltage Supply (V)	Supply Current (mA)	Temperature Range (°C)	Package	Status	Price* (1000-4999)
ADXL103	1	±1.7	1000 mV/*g*	±6	Analog	2.5	110	5 (3 to 6)	0.7	–40 to +125	E-8	Production	$7.75
ADXL203	2	±1.7	1000 mV/*g*	±6	Analog	2.5	110	5 (3 to 6)	0.7	–40 to +125	E-8	Production	$12.00
ADXL204	2	±1.7	620 mV/*g*	±5	Analog	2.5	170	3.3 (3 to 6)	0.5	–40 to +125	E-8	Production	$12.00
ADXL213	2	±1.2	30 %/*g*	±10	PWM	2.5	160	5 (3 to 6)	0.7	–40 to +85	E-8	Production	$9.70
ADXL320	2	±5	174 mV/*g*	±10	Analog	2.5	250	2.4 to 6	0.5	–20 to +70	CP-16	Production	$3.75
ADXL321	2	±18	57 mV/*g*	±10	Analog	2.5	320	2.4 to 6	0.5	–20 to +70	CP-16	Production	$3.75
ADXL322	2	±2	420 mV/*g*	±10	Analog	2.5	220	2.4 to 6	0.5	–20 to +70	CP-16	Production	$3.75
ADXL330	3	±2										Prerelease	
ADXL311	2	±2	174 mV/*g*	±15	Analog	6	300	2.4 to 5.25	0.4	0 to +70	E-8	Phase Out	$4.25
ADXL202	2	±2	12.5 %/*g*	±16	PWM	6	200	3 to 5.25	0.6	–40 to +85	E-8	Phase Out	$8.50
ADXL210	2	±10	4.0 %/*g*	±20	PWM	6	200	3 to 5.25	0.6	–40 to +85	E-8	Phase Out	$8.50

*The pricing listed here is provided only for budgetary purposes as recommended list price in U.S. dollars in the United States ex factor per unit for the stated volume. Pricing displayed for evaluation boards and kits is based on 1-piece pricing.

**Sensor bandwidth is set by the customer in the application.

This article can be found at http://www.analog.com/library/analogdialogue/archives/39-11/hdd.html, with a link to a PDF.

A Reference Design for High-Performance, Low-Cost Weigh Scales

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INTRODUCTION

The trend in weigh scales towards higher accuracy and lower cost has produced an increased demand for high-performance analog signal processing at low cost. The scope of this requirement is not obvious; most weigh scales output the final weight value at a resolution of 1:3,000 or 1:10,000, which is easily met (apparently) by a 12-bit to 14-bit ADC (analog-to-digital converter). However, a closer examination of weigh scales shows that meeting the resolution requirement is not that easily accomplished; in fact, the ADC accuracy needs to be closer to 20 bits. In this article, we discuss some of the system specifications of weigh scales and deal with considerations for designing and building a weigh-scale system. The main areas considered are peak-to-peak-noise resolution, A/D-converter dynamic range, gain drift, and filtering. We compare measured data from a real load cell to inputs from a stable voltage reference, using a weigh-scale reference design as an evaluation board.

Load-Cell Sensor

The most common weigh-scale implementation is to use a bridge-type load-cell sensor, with voltage output directly proportional to the weight placed on it. A typical load-cell bridge is illustrated in Figure 1; it is a 4-resistor bridge circuit with at least two variable arms, where the resistance change with weight applied creates a differential voltage at a common-mode level of 2.5 V (one-half the supply voltage). A typical bridge will have resistors of the order of 300 Ω.

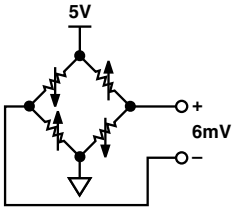

Figure 1. Basic circuit of load cell.

The load cell is inherently monotonic. The main parameters of the load cell are *sensitivity*, *total error*, and *drift*.

Sensitivity

A typical load cell's electrical sensitivity, defined as the ratio of the full-load output to the excitation voltage, is 2 mV/V. With 2-mV/V sensitivity and 5-V excitation, the full-scale output voltage is 10 mV. Often, in order to use the most linear portion of the load cell's span, only about two-thirds of this range would be used. The full scale output voltage would thus be about 6 mV. The challenge thus posed is to measure small signal changes within this 6-mV full-scale range in such a way as to get the highest achievable performance—not an easy task in the industrial environments where weigh scales would typically be used.

Total Error

The total error is the ratio of the output error to the rated output. A typical weigh scale has a total error specification of about 0.02%. It is a very important specification, because it limits the accuracy that could be reached with an ideal signal conditioning circuit. It thus determines the choice of A/D-converter resolution, as well as the design of the amplification circuit and filter.

Drift

Load cells also drift over time. Figure 2 shows an actual load-cell drift characteristic, measured over a 24-hour period. Temperature was essentially constant during the measurement period, so the drift is not temperature-related. The results show a total output drift of about 125 LSBs (as measured with a 24-bit ADC), or about 7.5 ppm.

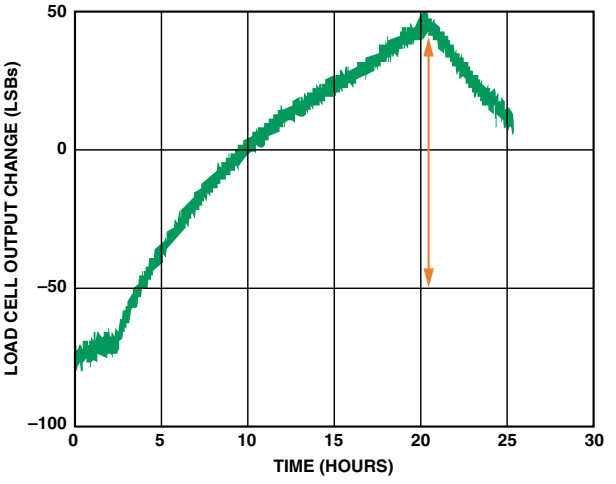

Figure 2. Long-term load-cell stability—24-hour plot.

Weigh-Scale System

The most important parameters to consider when designing a weigh-scale system are *internal count*, *ADC dynamic range*, *noise-free resolution*, *update rate*, *system gain*, and *gain-error drift*. The system must be designed to be *ratiometric*, hence independent of supply voltage—this will be discussed later.

Internal Count

As mentioned, the resolutions of typical weigh-scale systems, as seen by the user, range from a *count* of 1:3,000 at the low end up to 1:10,000 for high-end solutions. For example, a weigh scale that can measure up to 5 kilograms with a count of 1:10,000 has a weight resolution of 0.5 grams. This resolution, as seen on the LCD display, is generally referred to as the *external* count. In order to guarantee that this resolution is met accurately, the *internal* resolution of the system must be better by at least an order of magnitude. In fact, some standards dictate that the internal count of the system be a factor of 20 times better than that of the external count. For the example above, the internal count would need to be 1:200,000.

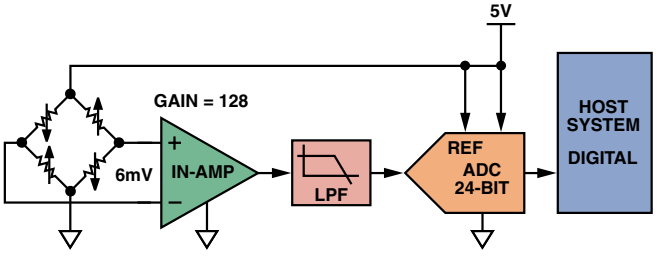

Figure 3. Typical weigh-scale system.

ADC Dynamic Range

In weigh-scale applications using standard high-resolution A/D converters, the entire full-scale range of the ADC is unlikely to be used. In the example of Figure 1, the load cell has a 5-V supply and a full-scale output of 10 mV. The linear range is 6 mV. Using a gain-of-128 stage on the front end, the ADC input will see about 768 mV full-scale. If a standard 2.5-V reference is used, only 30% of the ADC's dynamic range is used.

Table I. Output RMS Noise (μV) vs. Gain and Output Update Rate for the AD7799 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	0.64	0.6	0.185	0.097	0.075	0.035	0.027	0.027
8.33 Hz	1.04	0.96	0.269	0.165	0.108	0.048	0.037	0.040
16.7 Hz	1.55	1.45	0.433	0.258	0.176	0.085	0.065	0.065
33.3 Hz	2.3	2.13	0.647	0.364	0.24	0.118	0.097	0.094
62.5 Hz	2.95	2.85	0.952	0.586	0.361	0.178	0.133	0.134
125 Hz	4.89	4.74	1.356	0.785	0.521	0.265	0.192	0.192
250 Hz	11.76	9.5	3.797	2.054	1.027	0.476	0.326	0.308
500 Hz	11.33	9.44	3.132	1.773	1.107	0.5	0.413	0.374

Table II. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7799 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	23 (20.5)	22 (19.5)	22.5 (20)	22.5 (20)	22 (19.5)	22 (19.5)	21.5 (19)	20.5 (18)
8.33 Hz	22 (19.5)	21.5 (19)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	20 (17.5)
16.7 Hz	21.5 (19)	20.5 (18)	21.5 (19)	21 (18.5)	21 (18.5)	21 (18.5)	20 (17.5)	19 (16.5)
33.3 Hz	21 (18.5)	20 (17.5)	21 (18.5)	20.5 (18)	20.5 (18)	20.5 (18)	19.5 (17)	18.5 (16)
62.5 Hz	20.5 (18)	19.5 (17)	20.5 (18)	20 (17.5)	19.5 (17)	19.5 (17)	19 (16.5)	18 (15.5)
125 Hz	20 (17.5)	19 (16.5)	20 (17.5)	19.5 (17)	19 (16.5)	19 (16.5)	18.5 (16)	17.5 (15)
250 Hz	18.5 (16)	18 (15.5)	18.5 (16)	18 (15.5)	18 (15.5)	18.5 (16)	18 (15.5)	17 (14.5)
500 Hz	18.5 (16)	18 (15.5)	18.5 (16)	18.5 (16)	18 (15.5)	18.5 (16)	17.5 (15)	16.5 (14)

Figure 4. Equivalent input noise and resolution of the AD7799 A/D converter.

If the internal count needs to be 1:200,000 accurate for the full-scale range of 770 mV, the ADC therefore needs to be of the order of 3× to 4× better in order to meet the performance requirements. In this case, for a count of 1:800,000, the ADC would require 19 bits to 20 bits of accuracy. The practical challenge posed by the signal-processing requirement can now be understood.

Gain and Offset Drift

Industrial weigh-scale systems typically operate over a 50-degree (Celsius) temperature range. Designers must consider the accuracy of the system at temperatures beyond room temperature, since *gain drift* with temperature can be a dominant source of error. For example, a 20-bit stable system with a 1-ppm/°C gain-error drift will have 50 LSBs of error over a 50-degree range. Even though the system may be 1-LSB stable at 25°C, it is, in effect, only 50-LSBs accurate over the full temperature range. Choosing an ADC with low gain drift is thus a very important consideration when designing weigh scales.

Offset drift is not as big a consideration. Most sigma-delta ADCs are designed with inherent chopping-mode techniques, which give the advantage of lower drift and better immunity to 1/f noise—useful features for weigh-scale designers. For example, the AD7799[1] A/D converter has an offset drift specification of 10 nV/°C. In a 20-bit system, this would contribute a total of only ¼-LSB error over the full 50-degree operating range.

Noise-Free Resolution

One common mistake when reading data sheets is lack of attention as to whether noise is specified as root mean square (rms) or peak-to-peak (p-p). For weigh-scale applications, the most important specification is p-p noise, which determines *noise-free-code resolution*. The noise-free-code resolution of an ADC is the number of bits of resolution beyond which it is impossible to distinctly resolve individual codes due to the effective input noise—associated with all ADCs. This noise can be expressed as an rms quantity, often as a number of LSB units (*counts*, 2^{-n} of full scale). Multiplying by 6.6 (to capture 99.9% of all values in a standard distribution) provides a reasonable approximation of the peak-to-peak noise (expressed in LSBs). Data sheets for most Analog Devices sigma-delta ADCs specify both the rms- and the p-p, or noise-free, codes, as shown in the table above, excerpted from the AD7799 data sheet.

Update Rate

In Figure 4, it can be seen that the noise-free resolution of the system depends on the update rate of the ADC. For example, using a 2.5-V reference and an update rate of 4.17 Hz, the resolution is 20.5 bits p-p (gain of 128); whereas at 500 Hz, the resolution decreases to 16.5 bits. In weigh-scale systems, the designer needs to balance the lowest update rate at which the ADC can be sampled with the output data rate needed to update the LCD display. For high-end weigh scales, a 10-Hz ADC update rate is generally used.

Weigh-Scale Reference Design

Choosing the Best ADC

The best ADC architecture to use for weigh-scale applications is sigma-delta, due to its low noise and its high linearity at low update rates. A further benefit is that noise shaping and digital filtering are implemented on-chip. The integration in the high-frequency modulator shapes the quantization noise so that the noise is pushed toward one half of the modulator frequency. The digital filter then band-limits the response to a significantly lower frequency. This greatly reduces the need for complex post-processing of the ADC data by the user.

The ADC should also contain a low-noise programmable-gain amplifier (PGA) with high internal gain to magnify the small output signal from the load cell. An integrated PGA can be optimized to give low temperature drift, as compared to a discrete amplifier with external gain resistors. With a discrete configuration, any errors due to temperature drift will get amplified through the gain stage. The AD7799, specifically designed for weigh-scale applications, has an excellent noise specification (27 nV/$\sqrt{\text{Hz}}$) and a front-end gain stage with a maximum gain of 128 mV/mV. The load cell can be directly interfaced to this ADC.

Figure 5 is a block diagram of a reference design, a weigh-scale system evaluation board designed at Analog Devices. It consists of an AD7799 ADC, controlled by an ADuC847[2] microcontroller. Besides providing the digital interface to the AD7799 and implementing the post processing, the ADuC847 microcontroller itself also contains a 24-bit, high-performance sigma-delta ADC. This will allow users to compare test results between a system containing the AD7799 ADC, and a completely self-contained system using the ADuC847 ADC, with the same hardware connections, so as to choose a design that best meets the requirements.

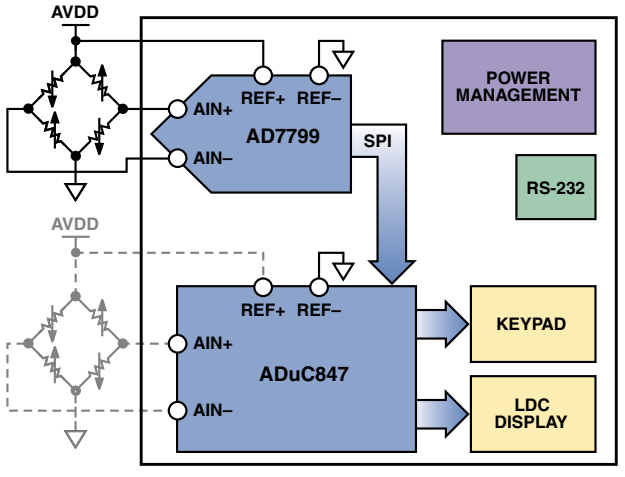

Figure 5. Reference-design block diagram.

Test Results

The following plots show some test results using the weigh-scale reference design. All results are based on the standard deviation of the measured ADC output codes, effectively the rms noise. To convert to "noise-free-resolution codes" we use the following calculation:

Standard deviation	=	rms noise (LSBs)
Peak-to-peak noise	=	6.6 × rms noise (LSBs)
Noise in bits of resolution	=	$\log_2$ (p-p noise)
ADC noise-free resolution (bits)	=	24 – (noise in bits)

$$= 24 - \log_2 (6.6 \times \textit{rms noise}\ (\text{LSBs}))\ \text{bits of resolution}$$

Figure 6 shows the measured data using the voltage reference as the input to the ADC. The standard distribution of the measured reference is 3.25 LSBs. Multiplying this by 6.6 to calculate the peak-to-peak noise gives 21.65 LSBs. Converting this into bits of resolution gives 4.42-bit noise. For a 24-bit ADC, this means 19.58 bits of "noise-free resolution." Figure 7 shows the same test completed on a typical load cell. The "noise-free resolution" in this case is 19.4 bits. This means that the load cell itself adds only 0.2 bits of noise to the final result, so the ADC is shown as the principal contributor of this noise.

Improving the ADC Result

The low-bandwidth, high-resolution AD7799 has a resolution of 24 bits. However, as shown above, the effective number of bits is limited by noise, depending on the output word rate and the gain setting used. In order to increase the effective resolution and

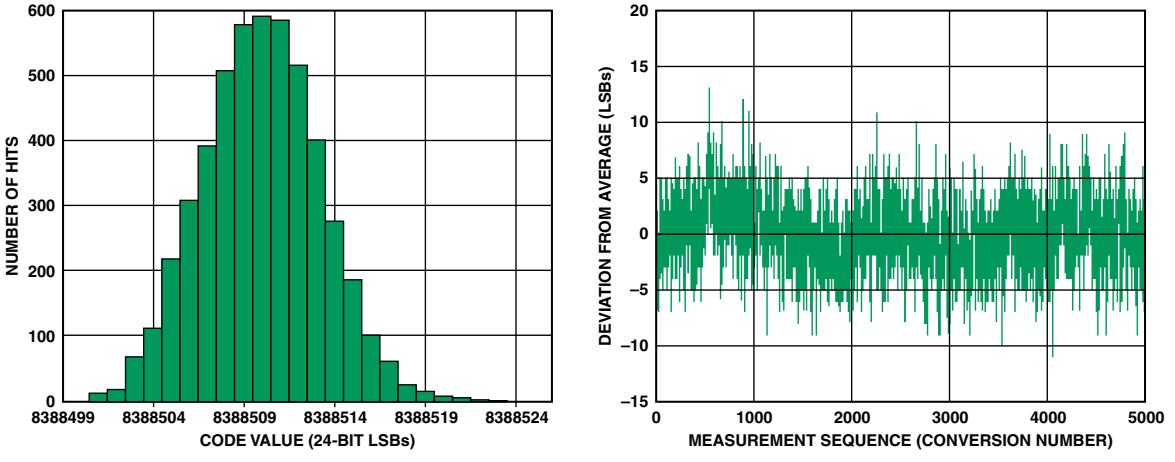

Figure 6. AD7799 noise performance at: gain = 64, update rate = 4.17 Hz, reference = 5 V, inputs shorted to the reference. RMS noise = 3.2526 LSBs, p-p resolution = 19.576 bits.

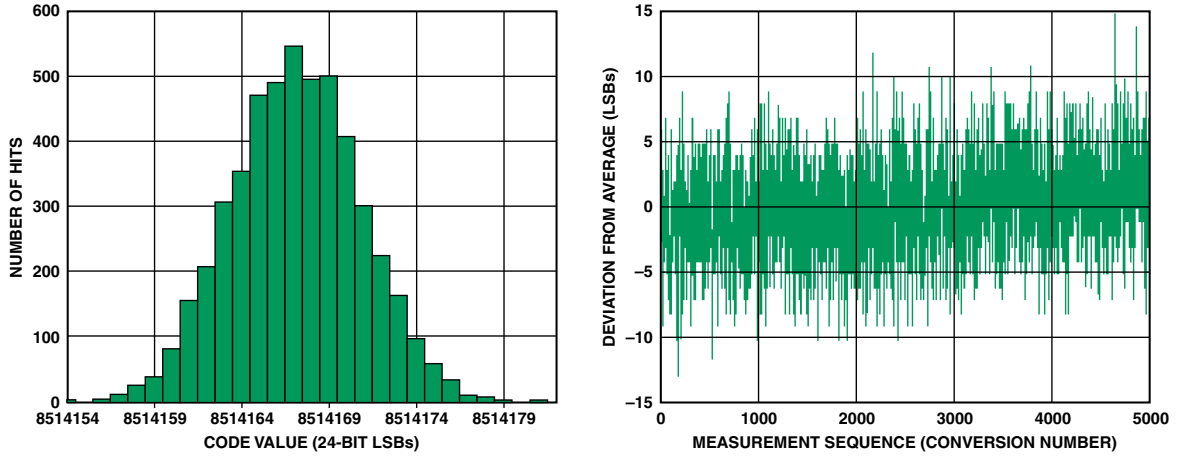

Figure 7. AD7799 noise performance at: gain = 64, update rate = 4.17 Hz, reference = 5 V, load-cell input. RMS noise = 3.6782 LSBs, p-p resolution = 19.399 bits.

remove as much noise as possible, the ADuC847's microcontroller was programmed to employ an averaging algorithm to get better performance. Figure 8 shows a typical histogram obtained from a sigma-delta ADC when the analog input is grounded. Ideally, for this fixed dc analog input, the output code should be constant. However, due to noise, there will be a spread of codes around the constant analog input value. This noise is due to thermal noise within the ADC and quantization noise inherent in the analog-to-digital conversion process. The code spread is generally Gaussian in nature.

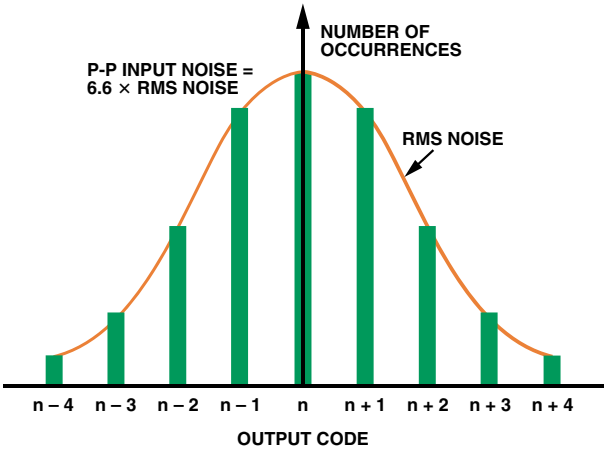

Figure 8. Histogram for an ADC measuring a constant analog input.

An averaging filter is a good way to reduce random white noise while keeping the sharpest step response. The software for the design discussed here uses a moving-averaging algorithm. Figure 9 shows the basic algorithm flow.

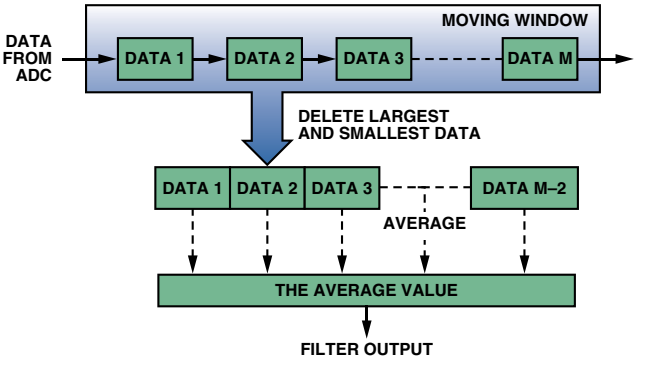

Figure 9. Averaging algorithm.

A moving-average filter averages a number of points from the input signal to produce each point in the output signal. The input to the filter is taken directly from the ADC. Operating on the most recent M data points, the smallest and the largest data points (the outliers) are deleted from the data window. The remaining M – 2 points are averaged, as shown in the equation.

$$y[i] = \frac{1}{M-2}\sum_{j=0}^{M-3} x[i+j]$$

Using the moving-average technique, the output data rate remains the same as the input data rate. This is first-order averaging. For higher update rates, second-order averaging is generally used to reduce the waveform dispersion. In that case, the output from the first stage is averaged through a second stage to further improve results.

Figure 10 shows the measured data from the AD7799 after averaging. Comparing this to Figure 5: after averaging there is

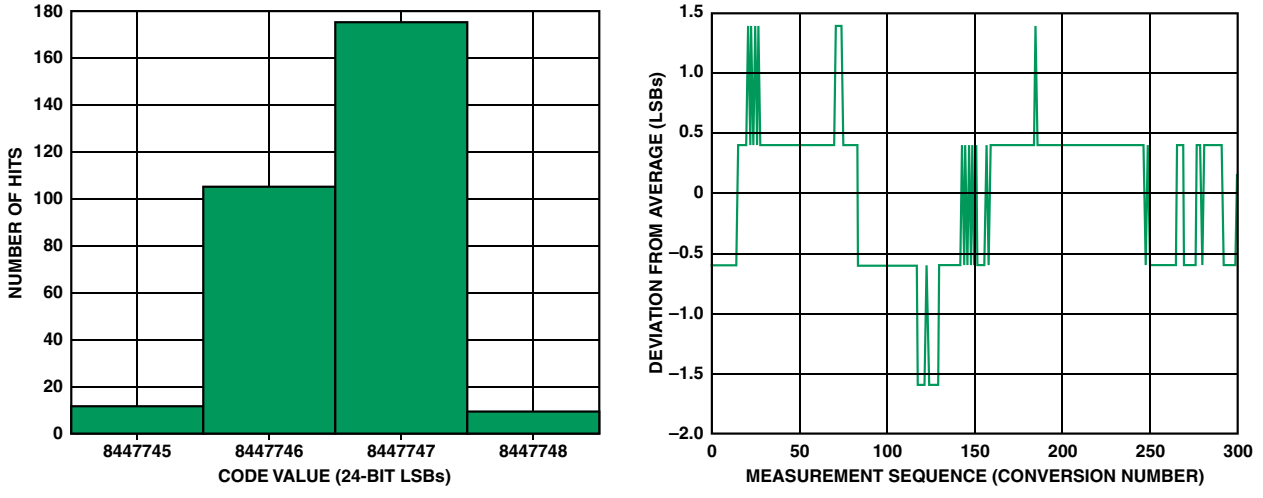

Figure 10. AD7799 noise performance after filtering at: gain = 64, update rate = 4.17 Hz, reference = 5 V, load-cell input. RMS noise = 0.611 LSBs, p-p resolution = 21.9 bits.

an improvement of about 2.3 bits in the final result (21.9-bit vs. 19.6-bit effective resolution). This technique can dramatically improve the final result, with no effect on LCD-output update rate. The only disadvantage of this technique is a longer settling time due to the pipeline delay of the averaging.

Improving the Response Time to Weight Changes

The basic algorithm can improve the noise performance, but it has a problem when the weight is changed. After a weight change, the output of the load cell should move to another balanced state in a very short time. According to the algorithm, the output of the filter can only indicate the most correct result after the filter refreshes M times. The response time is limited by the number of averaging points. A specific algorithm is needed to judge the change of the weight. Figure 11 shows the basic flow of this algorithm.

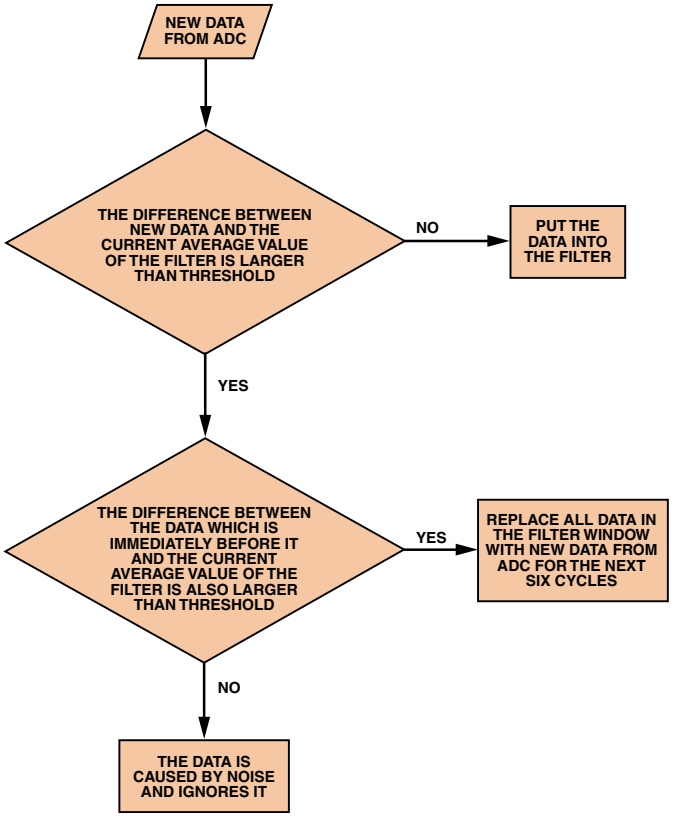

Figure 11. Weight-change judgment algorithm.

First, doubled judging steps are used in order to avoid taking a glitch as a weight change. When the differences between two continuous data points from the ADC and the output of the filter both exceed the threshold, this is considered as a weight change. All *M* points of the second stage will be filled with the same new data in order to skip the transition period of the load cell very quickly after weight change. Also, the load cell itself has a settling time. To compensate for this, after a weight change is detected, all the data in the averaging moving window will be refreshed with the newest ADC data for the next six continuous averaging cycles to pass the recovery time by. After the six refreshing cycles, the averaging will resume.

Removing Flicker on the Output Result

The weigh scale is aligned to display 0.5-gram divisions or 1-gram divisions for 1:5,000 and 1:10,000 standard ranges. When the weight is in the margin between two adjacent display weights, the display will flicker between these weights. In order to keep the display stable, the algorithm in Figure 12 is used:

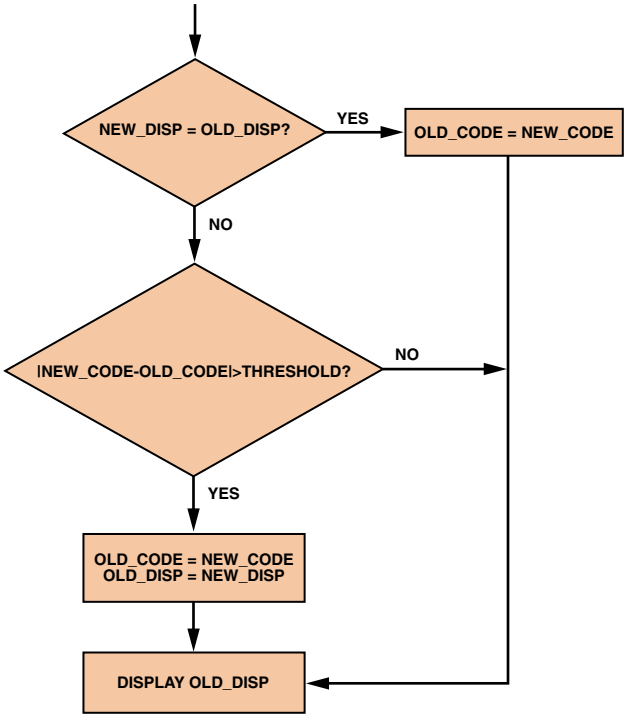

Figure 12. Code-change flow chart.

In every display cycle, the software decides whether the displayed weight in this cycle is the same as the previous one. If it is the same, the LCD output will not change and the process continues to the next cycle. If it is different, the internal code difference between these two cycles will be calculated. If the difference is smaller than the threshold, it is regarded as noise effect, so the old weight will still be displayed. If the difference is bigger than the threshold, it will update the display.

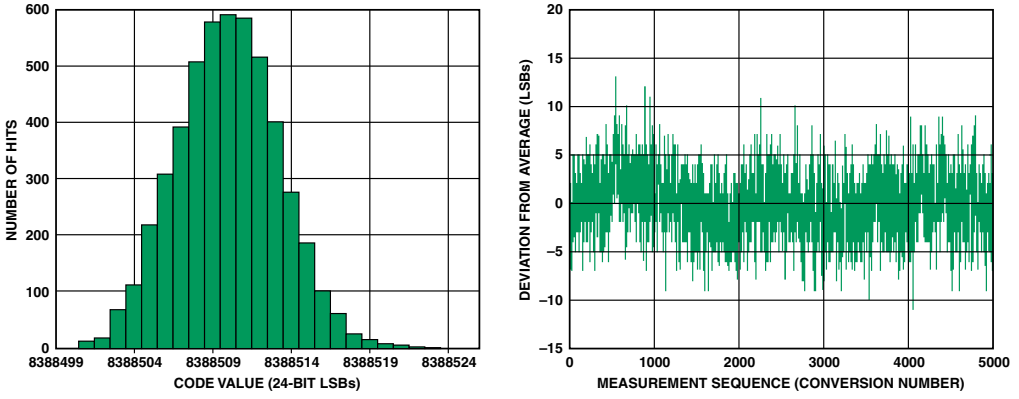

Figure 13. AD7799 noise performance: gain = 64, update rate = 4.17 Hz, reference = 5 V, inputs shorted to reference. RMS noise = 3.2526 LSBs, p-p resolution = 19.576 bits.

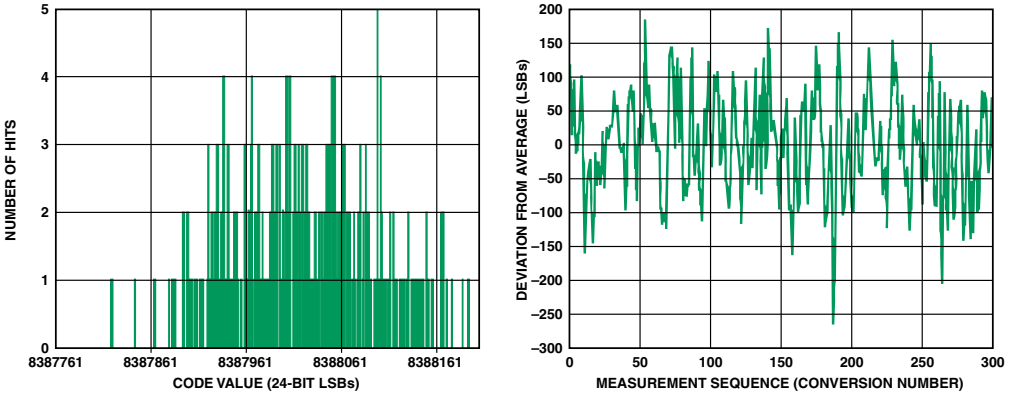

Figure 14. ADuC847 noise performance: gain = 64, update rate = 5.35 Hz, reference = 2.5 V, inputs are shorted to reference. RMS noise = 74.65 LSBs, p-p resolution = 15 bits, data sheet spec = 15 bits.

Comparing ADuC847 and AD7799 ADC Performance

For low-cost weigh-scale design, the ADuC847, with its on-board ADC, can provide a single-chip solution. The ADuC847 integrates a 24-bit sigma-delta ADC and an 8052 microcontroller core. The internal ADC also has a gain-of-128 PGA with differential analog inputs and reference inputs. It also includes 62K bytes of on-chip program flash memory and 4K bytes of on-chip data flash memory. The plots in Figures 13 and 14 compare the integrated ADC on the ADuC847 with the lower noise standalone AD7799. The conditions for both tests are the same: analog inputs are shorted to the 2.5-V reference and a gain of 64 is used. As we would expect, the AD7799 has lower noise and so is suitable for high-end applications, whereas the ADuC847 would be suitable for less demanding weigh scales.

Weigh-Scale Design Considerations

Ratiometric Design

For best performance, ratiometric measurement techniques (same reference source for bridge excitation and ADC reference) are employed in the reference design, as in Figure 3. The output accuracy of the load cell is determined by the excitation voltage of the bridge. The bridge output is directly proportional to the excitation voltage, and any drift in the excitation voltage produces a corresponding drift in the output voltage. By using a voltage that is proportional to the bridge excitation voltage as the ADC's reference source, there is no loss in measurement accuracy if the actual bridge excitation voltage varies. This *ratiometric* connection removes the effect of drifts and very low-frequency noise in the excitation source. In order to filter out noise from the load cell at the inputs to the ADC, a simple first-order RC filter can be used.

Layout

Layout[3] is very critical for best noise performance using a high-precision sigma-delta ADC. The most important two aspects are grounding and power-supply decoupling. In this reference design, the ground plane is separated into analog- and digital sections. The AD7799 sits above the split between these two ground planes. One starting point is used to connect the ground planes just under the AD7799. The GND pin of AD7799 should connect to the *analog* ground. In this design, just one power supply is used, but a ferrite bead goes between AVDD and DVDD terminals. The ferrite bead features low impedance at low frequencies and high impedance at high frequencies. Therefore, the ferrite bead blocks the high frequency noise in DVDD. When selecting a ferrite bead, one should investigate its impedance-vs.-frequency characteristic. In this design, a 600-Ω surface-mount-package ferrite bead is selected. Finally, 0.1-µF and 10-µF capacitors are used to decouple AVDD and DVDD supplies; they should be placed as closely as possible to the device.

Hardware and Software

The AD7799/ADuC847 weigh-scale reference design can also be interfaced to any PC, using an RS-232 interface. This allows the user to save and process data when evaluating the system. The hardware and software specifications of the reference design are freely available, including source code, schematic, and PCB Gerber files. Please contact the authors for more information.

REFERENCES—VALID AS OF JANUARY 2006

[1] ADI website: www.analog.com (Search) AD7799 (GO)
[2] ADI website: www.analog.com (Search) ADuC847 (GO)
[3] http://www.analog.com/library/analogdialogue/archives/39-09/layout.html

This article can be found at http://www.analog.com/library/analogdialogue/archives/39-12/weigh_scale.html, with a link to a PDF.

PRODUCT INTRODUCTIONS: VOLUME 39, NUMBER 4

Data sheets for all ADI products can be found by entering the model number in the Search Box at www.analog.com

October

ADC, Successive-Approximation, 16-bit, 1.33-MSPS **AD7623**
ADC, Sigma-Delta, 24-bit, 2.5-MSPS, 100-dB dynamic range, on-chip buffer **AD7760**
Amplifier, Operational, low-power, low-noise, low-distortion, rail-to-rail output .. **ADA4841-1**
CCD Signal Processor, with V-driver and *Precision Timing*™ generator **AD9923**
Clock Distribution IC, 1.6-GHz, triple-output **AD9514**
Clock Distribution IC, 1.6-GHz, dual-output **AD9515**
Comparators, Voltage, ultrafast SiGe **ADCMP580/ADCMP581/ADCMP582**
Controller, DC-to-DC, 20-A, step-down **ADP1821**
Controller, Synchronous Buck, 8-bit, 2-phase to 5-phase **ADP3189**
Controller/Monitor, avalanche photodiode, wide dynamic range **ADL5317**
DAC, Voltage-Output, 16-bit, buffered, SOT-23 package **AD5061**
DAC, Voltage-Output, 16-bit, unbuffered, SOT-23 package, 1-LSB INL **AD5062**
DAC, Current-Output, 16-bit, 400-MSPS, LVDS interface **AD9726**
DACs, Current-Output, dual, 12-/14-/16-bit, 1-GSPS, ... **AD9776/AD9778/AD9779**
Decoder, Video, 10-bit, multiformat SDTV, with fast switch-overlay support **ADV7184**
Decoder, Video, 12-bit, multiformat SDTV, with fast switch-overlay support **ADV7188**
Direct Digital Synthesizer, 2-channel, 10-bit, 500-MSPS **AD9958**
Energy Measurement IC, low-power, polyphase **ADE7752A**
Multiplexer/Demultiplexer, quad 2:1, 3.2-Gbps **AD8159**
Supervisory Circuit, low-voltage, includes watchdog and manual reset **ADM6823**

November

Accelerometer, Dual-Axis, ±1.7-*g*, SPI interface **ADIS16003**
ADC, Pipelined, dual, 12-bit, 65-MSPS **AD15252**
ADC, Sigma-Delta, 24-bit, 625-kSPS, 109-dB dynamic range, on-chip buffer **AD7762**
ADCs, Successive-Approximation, 10-bit/12-bit, 3-MSPS, 8-lead TSOT packages **AD7273/AD7274**
Amplifier, Variable-Gain, dc-coupled **AD8337**
Buffers, LCD Gamma-Reference, 4-/5-/6-channel, multiplexed-input **ADD8504/ADD8505/ADD8506**
Clock and Data Recovery ICs, 10-Mbps to 1.25-Gbps/675-Mbps, limiting amplifier **ADN2813/ADN2814**
Clock and Data Recovery ICs, 10-Mbps to 1.25-Gbps/675-Mbps **ADN2815/ADN2816**
Clock-Distribution IC, 800-MHz, triple-output **AD9513**
Controller, DC-to-DC, 20-A, step-down **ADP1822**
Controller, DC-to-DC, 20-A, step-down, with tracking and margining **ADP1822**
Controller, Secondary-Side, supports current sharing and housekeeping **ADM1041A**
Correlated Double Sampler, high-speed, integrated timing driver **AD9940**
DACs, Voltage-Output, 8-/10-/12-bit, I²C-compatible interface, SC70 package **AD5602/AD5612/AD5622**
DACs, Voltage-Output, 12-/14-/16-bit, 5-ppm/°C reference, SOT-23 package **AD5620/AD5640/AD5660**
Driver, Laser-Diode, 4-channel, dual-output with oscillator, supports 16× write speeds **AD9668**
Imaging Signal Processor, complete, 14-bit, 56-MSPS **AD9941**
Interface, Display, analog, 110-MSPS/140-MSPS **AD9985A**
Interface, Display, analog/HDMI **AD9880**
Isolators, Digital, quad, 5-kV **ADuM2400/ADuM2401/ADuM2402**
Temperature Sensor, Digital, 12-bit, ±1°C accuracy **ADT75**
Temperature Sensor, Digital, 13-bit, ±1°C accuracy **ADT7301**
Temperature Sensor, Digital, 13-bit, ±2°C accuracy **ADT7302**
Temperature Sensor, Digital, over-/undertemperature alarms **ADT7483A**

December

ADC, Pipelined, 14-bit, 105-MSPS/125-MSPS, IF-sampling **AD9945**
ADC, Pipelined, quad, 12-bit, 65-MSPS **AD15452**
ADC, Successive-Approximation, 8-channel, 12-bit-plus-sign **AD7328**
Amplifier, Operational, triple, 1.5-GHz, ultrahigh-speed, current-feedback **AD8003**
Amplifier, Operational, dual, low-noise, low-power, low-distortion, rail-to-rail outputs **ADA4841-2**
Amplifier, Operational, triple, low-cost, high-speed, current-feedback **ADA4861-3**
Amplifier, Operational, high-speed, ultralow noise and distortion **ADA4899-1**
Controller, DC-to-DC, step-down, constant-frequency current mode **ADP1864**
Controller, Thermoelectric-Cooler (TEC) **ADN8831**
Converter, Impedance-to-Digital, 12-bit, 1-MSPS **AD5933**
DACs, Voltage-Output, octal, 12-/14-/16-bit, 5-ppm/°C reference ... **AD5628/AD5648/AD5668**
DAC, Voltage-Output, quad, 16-bit, 5-ppm/°C reference **AD5666**
DAC, Voltage-Output, octal (4 × 12-bit and 4 × 16-bit), 5-ppm/°C reference **AD5678**
Demodulator/Phase Shifter, Quadrature, dual, dc-to-50-MHz **AD8333**
Detectors/Controllers, Logarithmic, 1-MHz to 10-GHz, 40-dB/50-dB dynamic range **AD8319/AD8317**
Driver, Video, triple, differential, sync-on-common-mode circuitry **AD8134**
Driver, ADC, low-distortion, high-voltage, differential **ADA4922-1**
Energy-Metering ICs, integrated oscillator and no-load indication **ADE7768/ADE7769**
Level Translator, 8-channel, CMOS logic levels to high-voltage logic levels **ADG3123**
Receiver, Cat-5, adjustable line equalization **AD8128**
Receiver, Video, triple, high-speed, differential **AD8143**
Switch, CMOS, dual SPDT, low-capacitance, low-charge injection, high-voltage **ADG1236**
Switches, CMOS, quad SPST, high-voltage **ADG1311/ADG1312/ADG1313**
Transceiver, RS-485/RS-422, half-duplex, slew-rate limited **ADM3493**
Transceivers, RS-485/RS-422, half- and full-duplex **ADM3483/ADM3485/ADM3488/ADM3490**

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