MicroZed SOM
Avnet Engineering Services
www.microzed.org

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01 - Avnet Lead Sheet
02 - Block Diagram
03 - DDR3
04 - QSPI FLASH, MicroSD
05 - ETHERNET, USB
06 - BANKS 34 and 35
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MicroZed SOM

3/22/2017

2:43:00 PM

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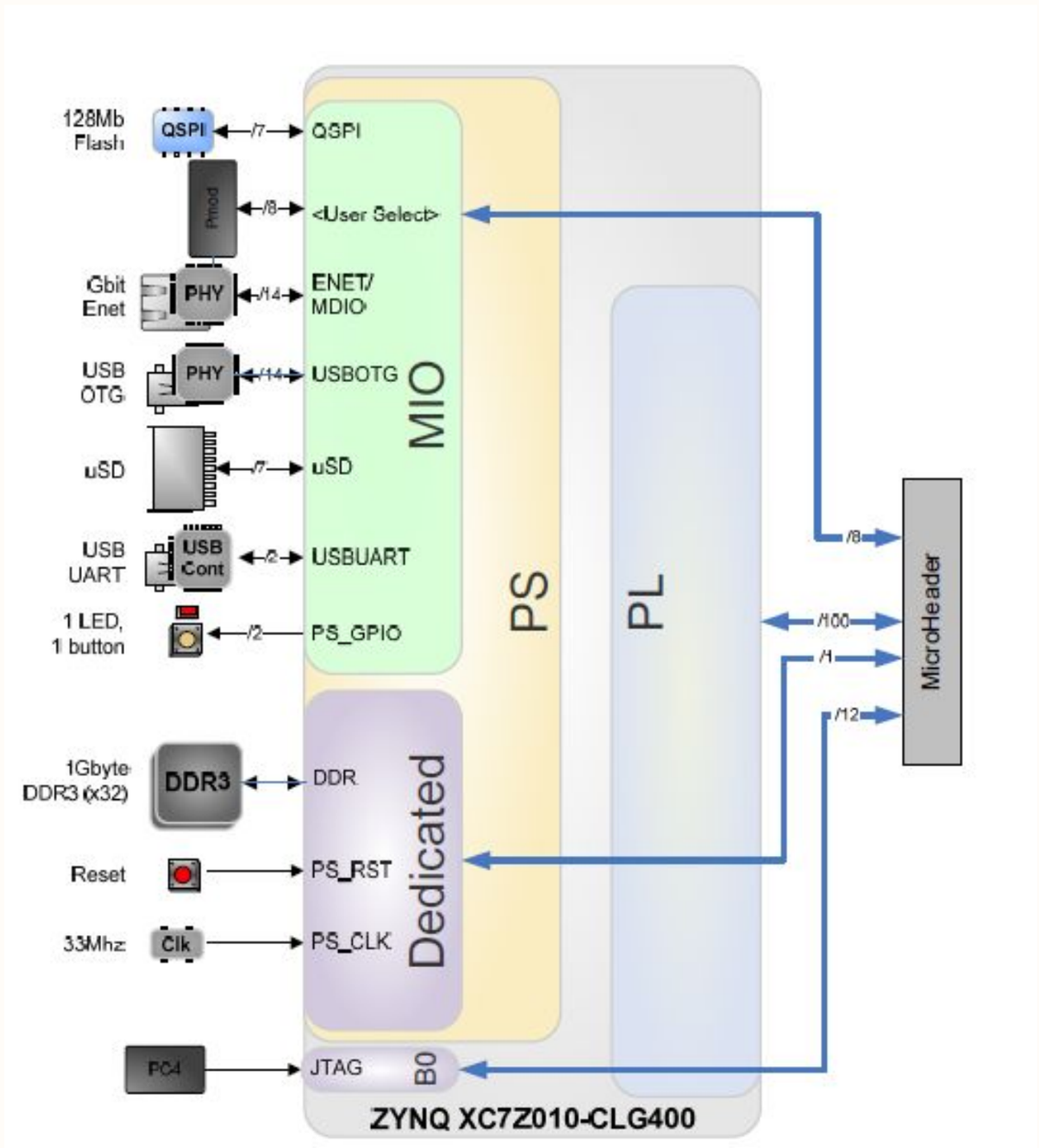

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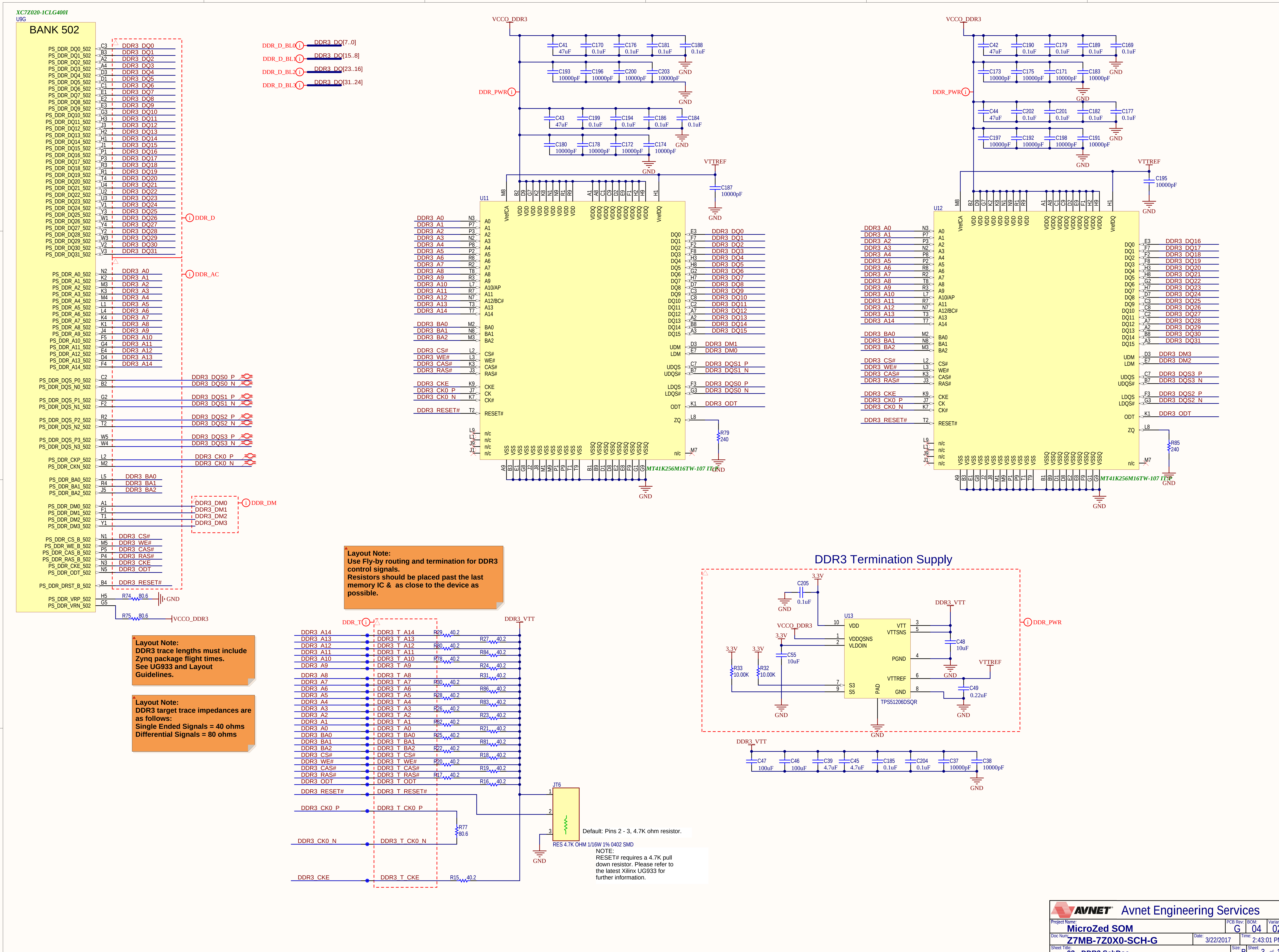
Sheet Title: 02 - Block Diagram.SchDoc	Size: B / Sheet: 2 of 11



XC7Z020-1CLG400I
U9G
BANK 502
DDR_D
DDR_AC
DDR_DM
DDR_D_BL0 DDR3_DQ[7..0]
DDR_D_BL1 DDR3_DQ[15..8]
DDR_D_BL2 DDR3_DQ[23..16]
DDR_D_BL3 DDR3_DQ[31..24]
VCCO_DDR3
DDR_PWR
VTTREF
GND
U11
U12
MT41K256M16TW-107 IT:P
R79 240
R85 240
R74 80.6
R75 80.6
DDR3 Termination Supply
U13
TPS51206DSQR
3.3V
DDR3_VTT
C205 0.1uF
C55 10uF
C48 10uF
C49 0.22uF
R33 10.00K
R32 10.00K
DDR_T
JT6
Default: Pins 2 - 3, 4.7K ohm resistor.
RES 4.7K OHM 1/16W 1% 0402 SMD
NOTE:
RESET# requires a 4.7K pull down resistor. Please refer to the latest Xilinx UG933 for further information.
R77 80.6
Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.
Layout Note:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.
Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms
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Sheet Title: 03 - DDR3.SchDoc
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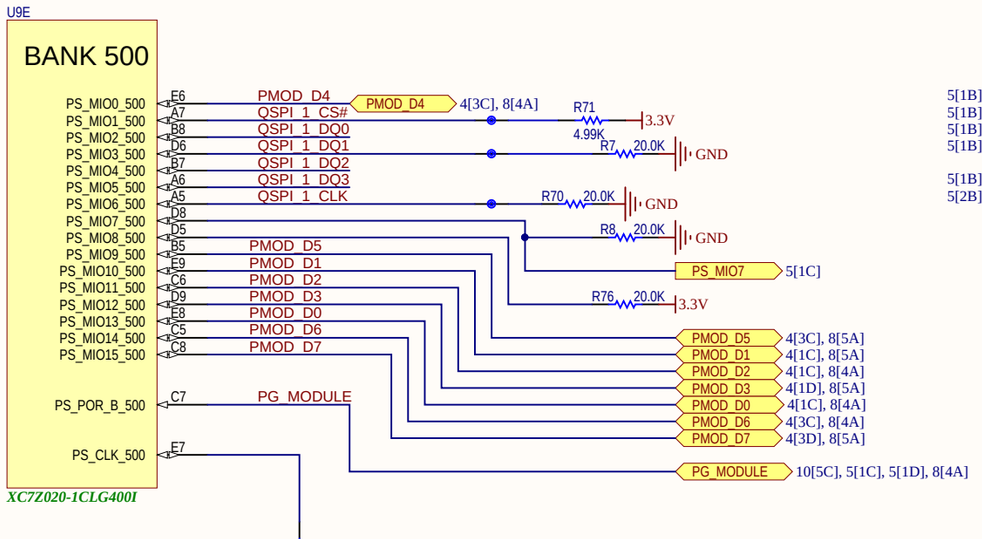

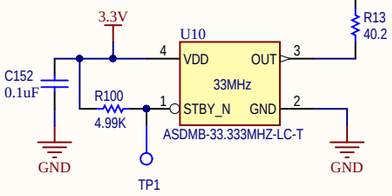

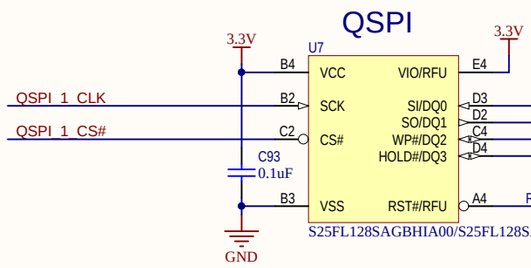

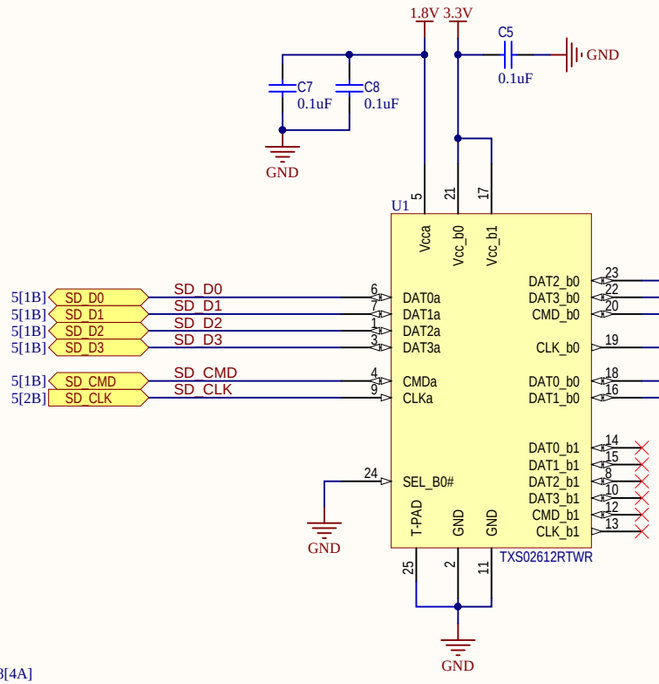

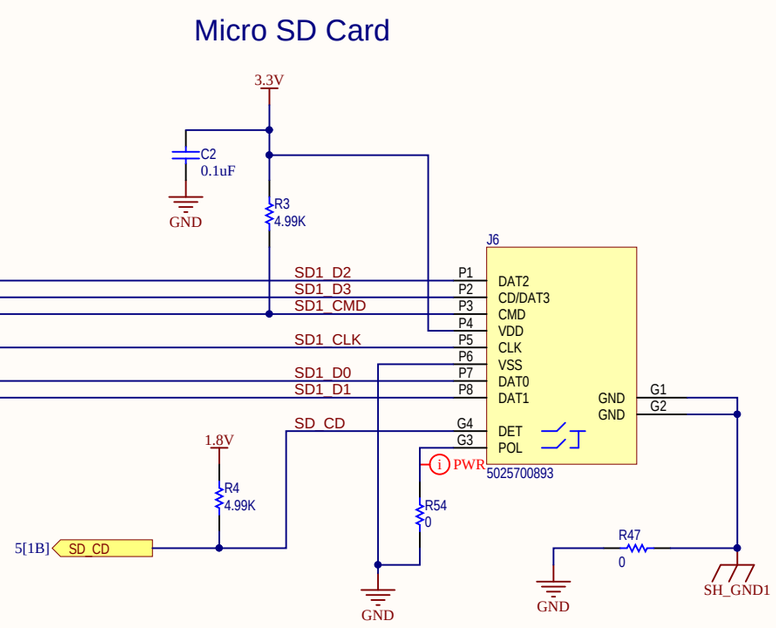

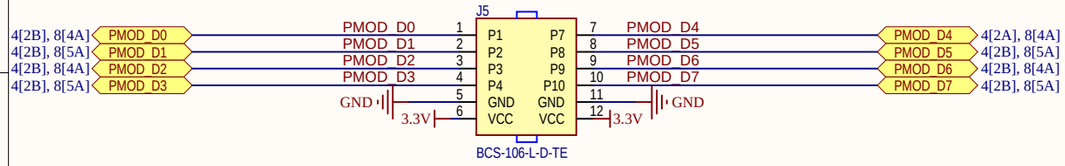

SHUNT, ECON, PHBR 15 AU,BLACK SHUNT, ECON, PHBR 15 AU,BLACK SHUNT, ECON, PHBR 15 AU,BLACK

Boot Mode:	JT1:	JT2:	JT3:
Cascade JTAG	1 - 2 (low)	1 - 2 (low)	1 - 2 (low)
Ind. JTAG	2 - 3 (high)	2 - 3 (high)	2 - 3 (high)
QSPI	x	1 - 2 (low)	2 - 3 (high)
SD Card	1 - 2 (low)	2 - 3 (high)	2 - 3 (high)

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Ethernet PHY

U9F
BANK 501
XC7Z020-1CLG400I

U3
88E1512-A0-NNP2I000

U9
RJ-45
USB-A
0821-1X1T-32-F

USB 2.0 OTG

U4
USB3320C-EZK

USB UART

U8
TXS0102DQER

USB LVL XNSLTR

U2
CP2104-F03-GM

ETH RESET DELAY & LVL XNSLTR

U21
SN74AHC1G08DBV

Layout Note:
USB differential signal impedance target is 90 ohms.

Layout Note:
USB_VBUS_OTG net must be 500mA or more capable.

Component Notes:
In USB Host Mode (default):
1) C1 & C3 required
2) R50 0603 0 Ohm or optionally a PTC can be placed

In USB Device Mode:
1) C1 & C3 not required
2) R50 Removed

R56:
Host/Device Mode = 10K
OTG Mode = 1K
Default = Host Mode.

Operational Notes:
USB Bus powered mode:
1) JT7 0 ohm pads 1-2.
2) DNP: D11, R97, R98.

USB Self powered mode:
1) JT7 0 ohm on pads 2-3.
2) R97, R98 populated.
3) DNP: D10, D11.

USB Self powered, no backfeed:
1) JT7 0 ohm on pads 2-3.
2) D10, D11 populated.
3) DNP: R97, R98.

NOTE: The components in the purple outlined areas MUST be placed if greater than +5.0 Vin is applied to the power jack! By Default these components are NOT placed and the board is powered via the USB UART port with +5.0V.

Layout Note:
USB_VBUS_UART net must be 1A or more capable.

Design Note:
R50 is a 0603 footprint. Generic PTCs can be placed, not to exceed 500mA withholding, can be a selectable PTC value, pending customer requirements.

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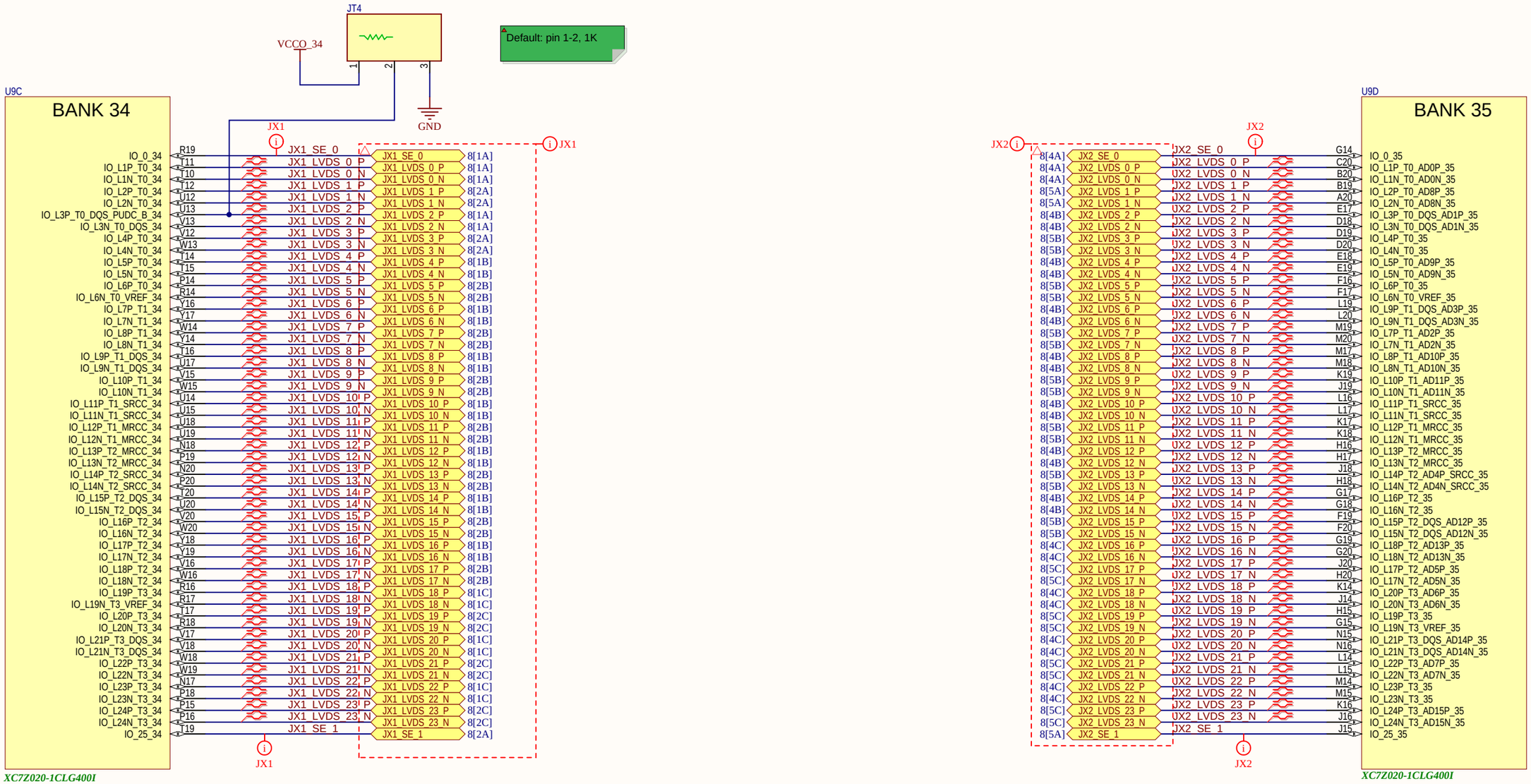

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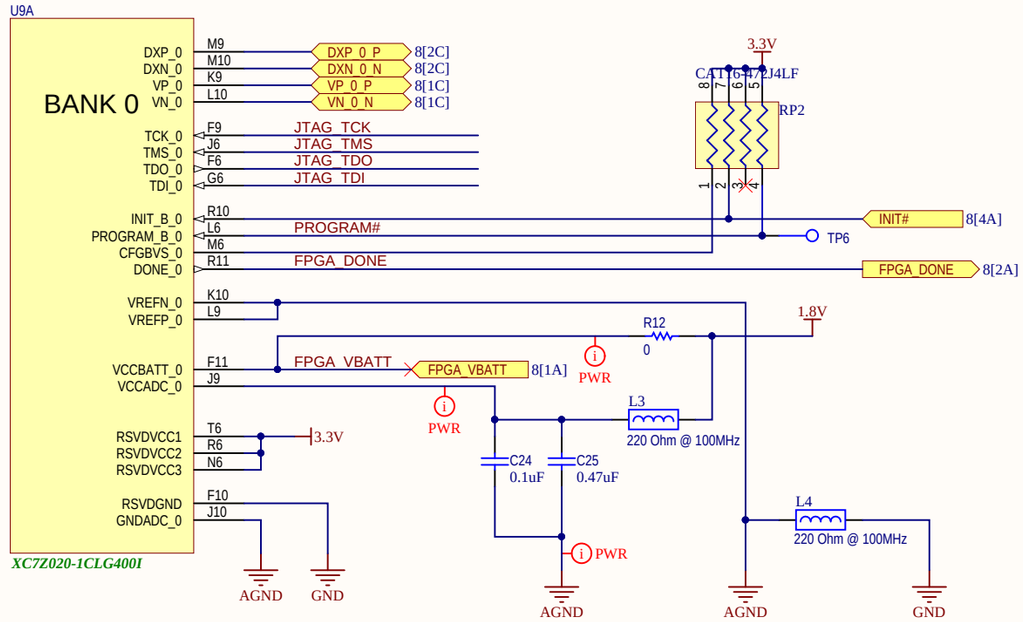

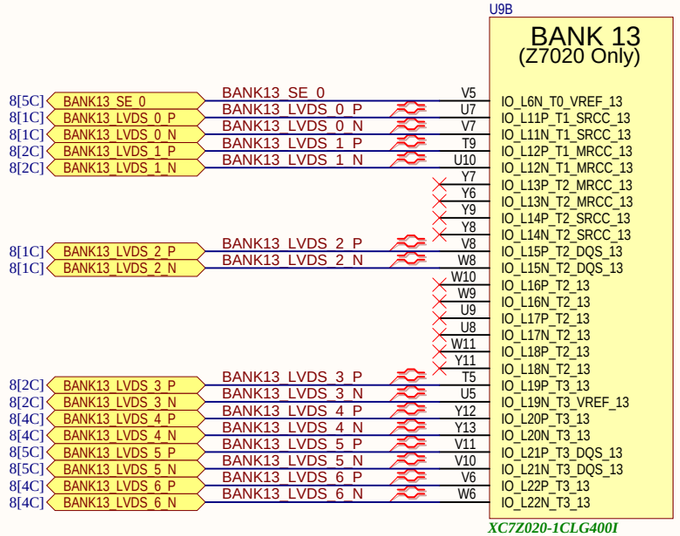

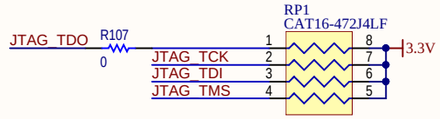

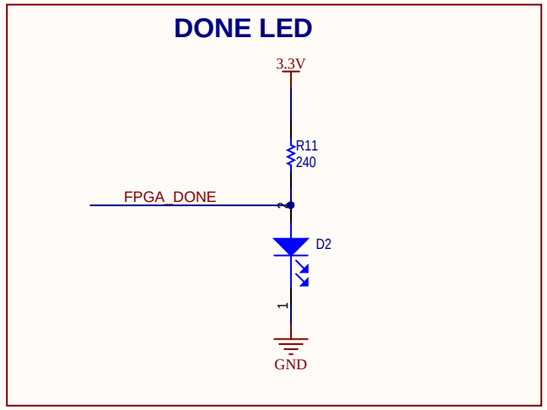

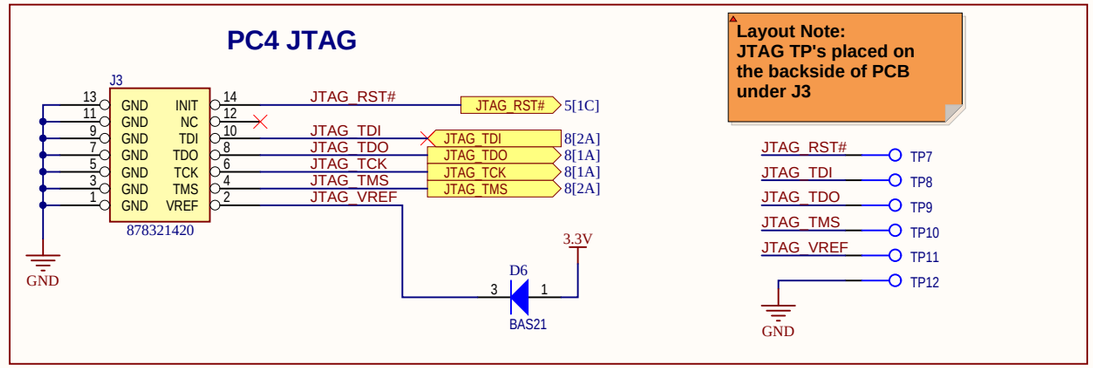

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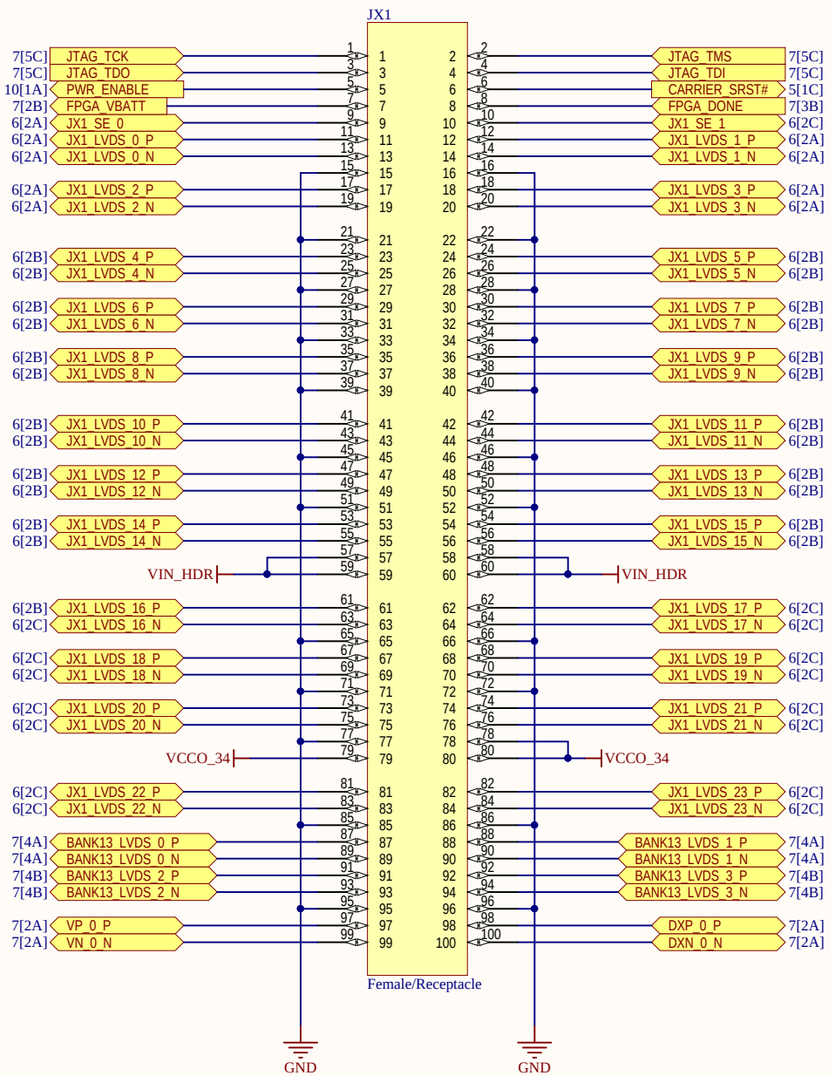

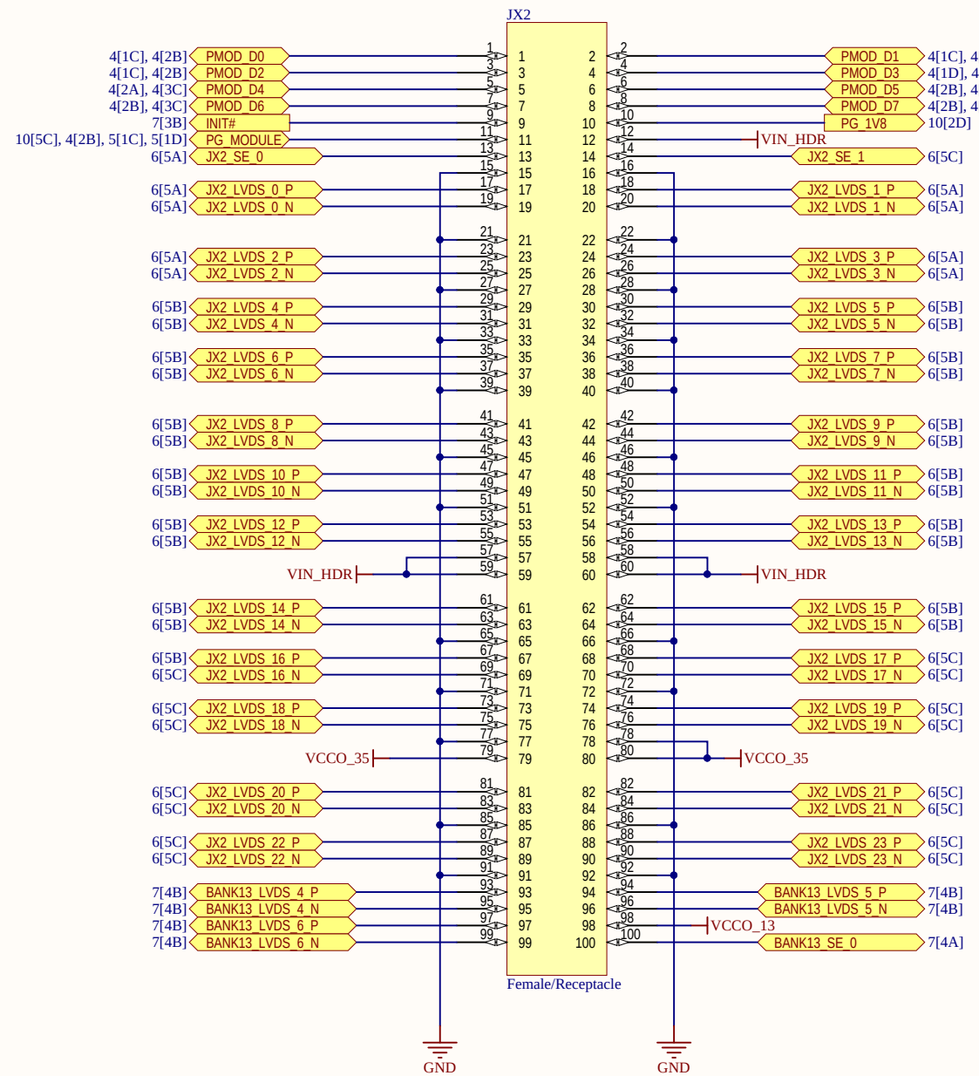

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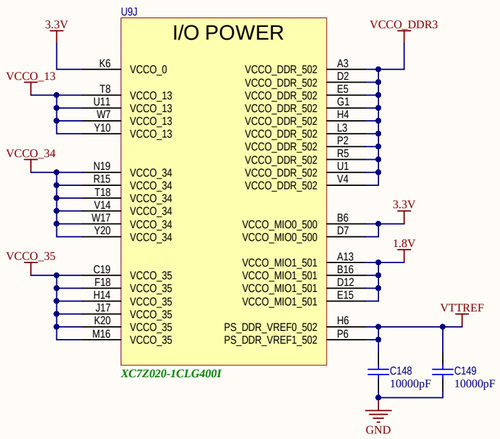
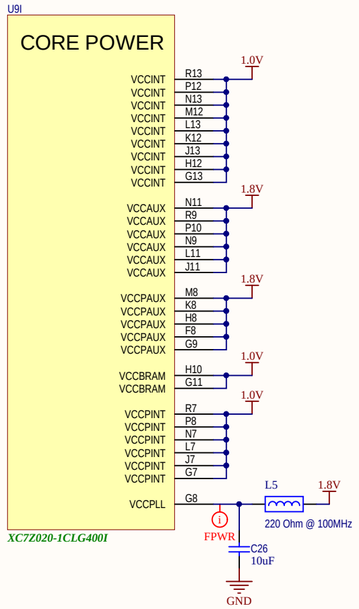
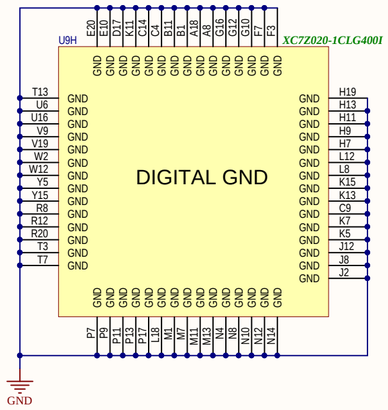
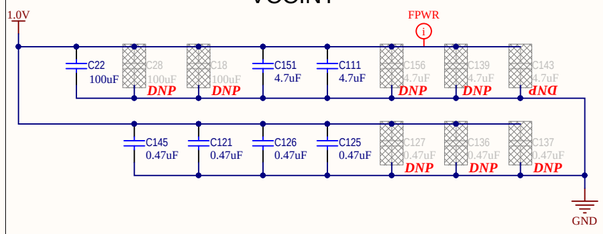


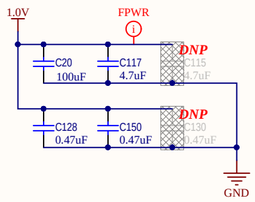




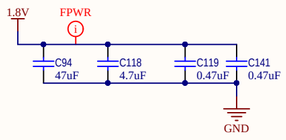
VCCINT



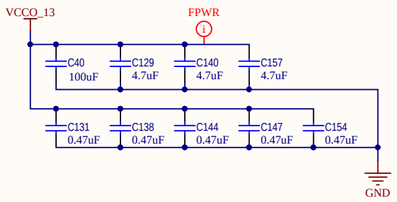
VCC_BRAM



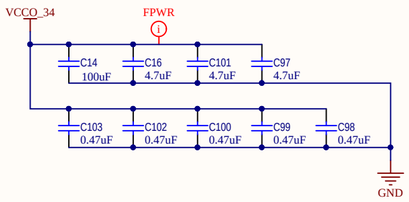
VCC_AUX



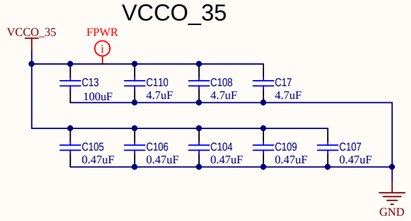
VCCO_13



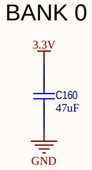
VCCO_34



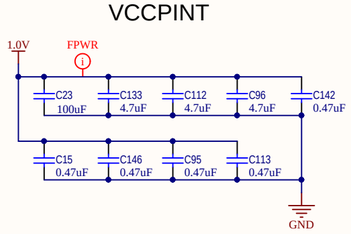
VCCO_35



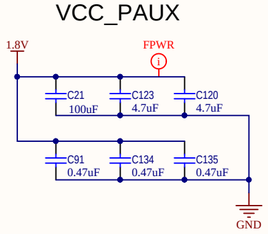
BANK 0



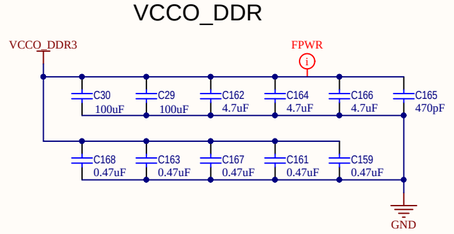
VCCPINT



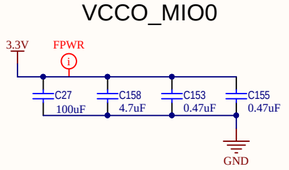
VCC_PAUX



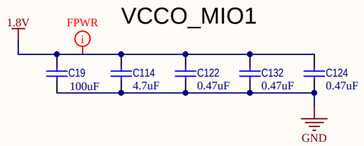
VCCO_DDR



VCCO_MIO0



VCCO_MIO1



VCC_PLL

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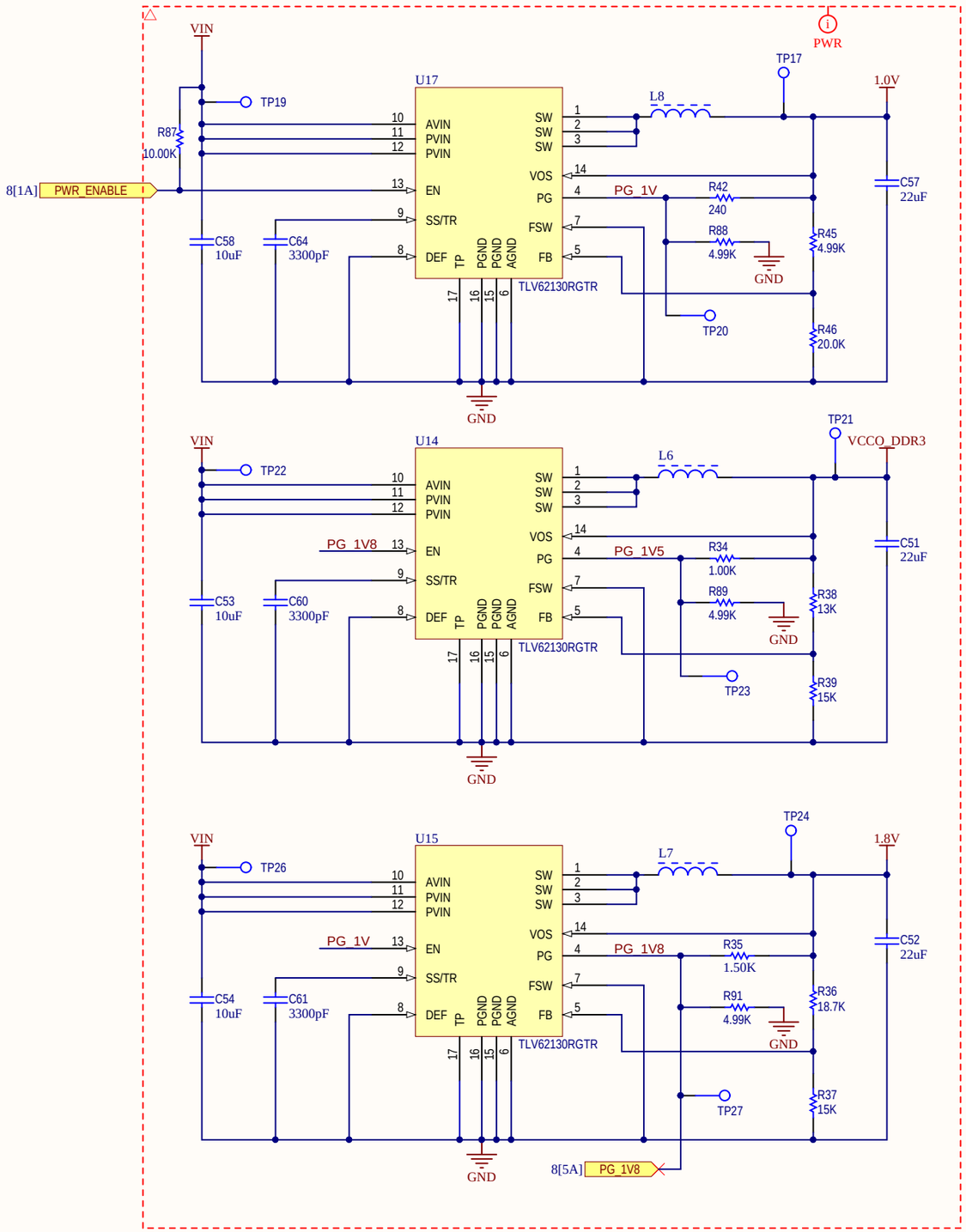

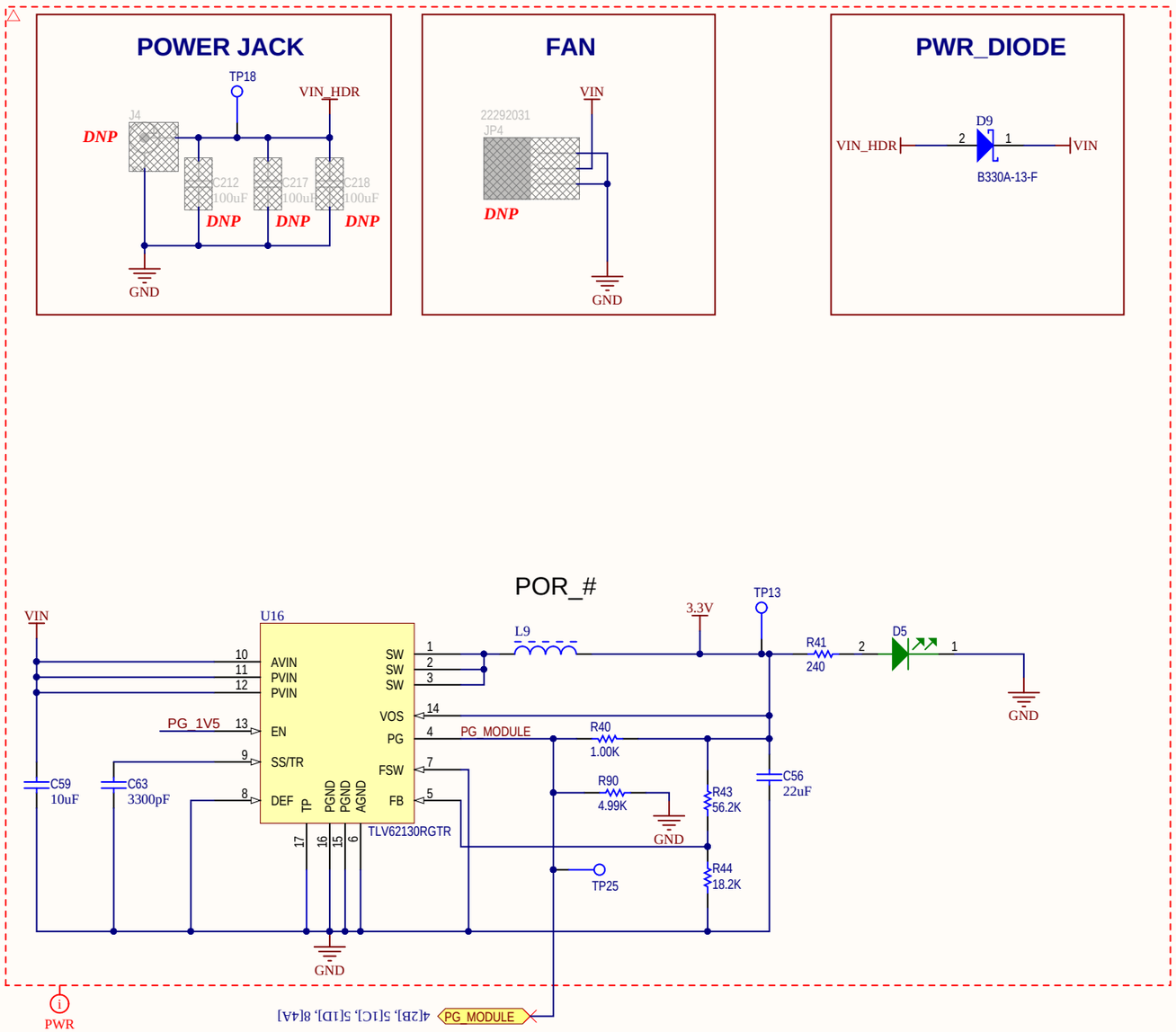

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Sheet Title: 10 - POWER, RESET.SchDoc		Size: B	Sheet: 10 of 11		

Revision Notes:

Revision C Changes:
1) Add Silkscreen Logos - CE, RoHS and Copper Part Number on board
2) Reduce R34, 35, (40), 42 from 100K to 1K
3) Add pulldown resistors to R34, 35, (40), 42 - Value 2.2K - 5.00K
4) Fuse (PTC) recommendation note for R50, 12V input
5) Connect: U8.6 to U20.2
6) Connect: U3.16 to U8.3
7) Connect: JX2.10 to U15.4
8) Change 4.75K resistors to 4.99K
9) Added rubber feet to BOM
10) Add staple point vias for J2 USB connector.

Revision D Changes (no production):
1) Attached JX2.10 to U15.4

Revision E Changes (no production):
1) Replaced U1 from MAX13035EETE+ to TI TXS02612ZQSR part.
2) Added Sheet 11.
3) Moved mechanical information to back page.

Revision F Changes:
1) Changed USB UART default power to bus power. Attach VBUS power net to U2.7 REGIN pin. Disconnect Vdd pin from +3.3V.
2) Added Ethernet LED drive buffer circuit to reduce 3.3V PHY backfeed.
3) Added: D10, D11, JT7, R97, R98 to allow user to configure USB Bus or Self power mode.
4) Removed two fansink mounting holes. Removed ground attribute to mounting holes (in layout files).
5) Added D12 PolyZen (PTC+Zen) USB UART protection component as configurable option.
6) Added R99 0 ohm resistor for D12 bypass (default).
7) Added C221 2.2uF capacitor for USB transient and flyback voltage protection.
8) Revised notes (above).
9) 28 Jan 14: Updated USB OTG configuration notes.
10) Updated JT6 note.

Revision G Changes:
1) Changed U13 VTT termination regulator pin 2 from 1.8V to 3.3V due to regulator back-feed.
2) Add Ethernet reset circuit to ensure a 10mS reset delay while board powers up.
3) Increase R71 to 4.99K
4) Added DFT/DFM hooks per CM recommendations.
5) Connect CP2104 VIO to VDD, named net Viousb and added TX/RX translators.
6) Add R111, R112 and connect RST to Viousb.
7) Add DNP R112 to PG_MODULE net for USB RESET_N.
8) Added JT to Ethernet PHY to allow address change.
9) Added 10uF cap to ETH AVDD18
10) Changed R35 to from 1.0K to 1.5K.
11) Changed Net 1.5V to VCCO_DDR3
12) Changed Net DDR3_0v75 to DDR3_VTT

Assembly:

Label1
BD-XXXX-XXXXX-G
Label, Product

Label2
XXXXXXX
Label, Serial Number

ESD1


ESD Bag

Label_ESD1


Label, ESD

Mechanicals:


PCB

PCB Mounting Holes

MTG5
Mounting Hole, 125mil

MTG2
Mounting Hole, 125mil

MTG1
Mounting Hole, 125mil

MTG6
Mounting Hole, 125mil

Fansink Mounting Holes

MTG4
0
Mounting Hole, 100mil

MTG3
0
Mounting Hole, 100mil

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